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Design Examples of Semiconductor Circuits

Edition 1974/75

SIEMENS AKTIENGESELLSCHAFT

The circuits described and suggested in this booklet are to demonstrate the manifold application possibilities for electronic components.

Similar applications have been grouped in chapters to offer a good survey.

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Contents

1. Rf- circuits

1.1 Medium-, short-, short-wave tuner with TCA 440

In principle the circuit shown in **fig. 1.1** is suitable for a receiver of short, medium or long waves. Instead of the latter range an additional short-wave band can be used.

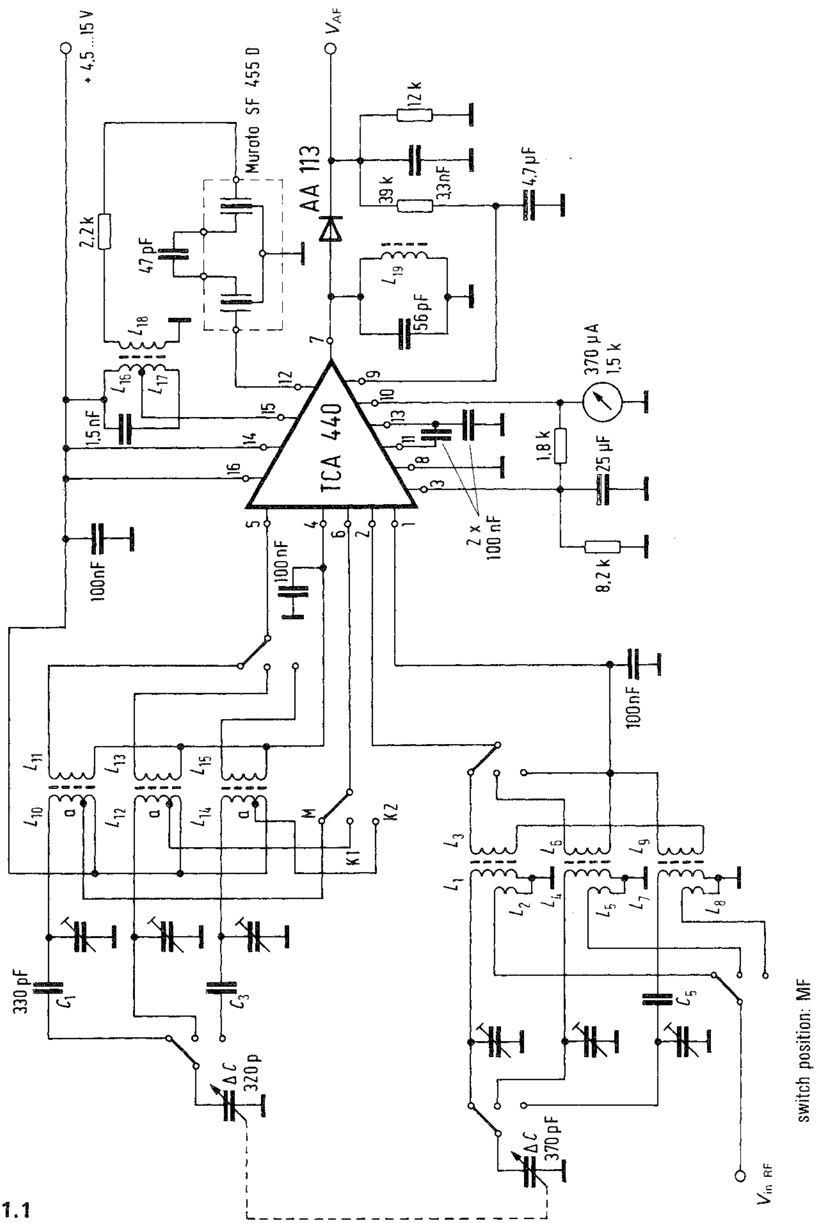


Fig. 1.1

As there exist different opinions upon the kind of switches which are to be used (rotary switch, slide switch or switching diodes) rotary switches were chosen.

The design example described shows an usual band-switching circuit for such a tuner. Dimensioning of two short-wave bands, for instance, can be made to the designers own ideas without considering the data indicated as below. The coil data for the medium-wave range are also given.

When designing the pc board it has to be taken care that neither parallel hot paths nor feedback circuits exist in order to avoid self-oscillation especially in the short-wave range. The padding capacitors, especially those of the short-wave range, enable the application of the AM-tuning diode BB 113 for this circuit, whereat also the circuits already discussed in Design Examples of Semiconductors, editions 73 and 74 can be used.

Data of coils

L_1	115 turns	12×0.04 CuL S
L_3	7 turns	0.10 CuL S
L_{10}	125 turns	12×0.04 CuL S
L_{17}	20 turns	12×0.04 CuL S
L_{18}	22 turns	12×0.04 CuL S
L_{19}	500 turns	0.04 CuL S
L_{10a}	35 turns	12×0.04 CuL S
L_{11}	15 turns	0.10 CuL S
L_{16}	50 turns	12×0.04 CuL S

L_1–L_3 Vogt kit D 21-2375.1
L_{10}–L_{11}–L_{16}–L_{19} Vogt kit D 41-2519

short wave ranges	circuit	C_S	C_P	circuit inductance
SW 1 4.5 to 12.5 MHz	r.f.-circuit	—	68 pF + timmer 3 to 12 pF	about 2.9 μH
	oscillator circuit	—	15 pF + timmer 3 to 12 pF	about 2.9 μH
SW 2 12 to 20 MHz	r.f.-circuit	150 pF	22 pF + timmer 3 to 12 pF	about 1.3 μH
	oscillator circuit	150 pF	22 pF + timmer 3 to 12 pF	about 1.2 μH

1.2 Short-wave tuner using BB 113 (5.8 to 10.5 MHz)

The short-wave tuner described below uses the Siemens triple-capacitance diode BB 113 and attains the same features as a conventional one with mechanical capacitors. The large signal behaviour is even better than that of the most transistorized mechanical varicap tuners. A silicon transistor BF 324 acts as mixer and the BF 450 as oscillator.

Fig. 1.2 shows a short-wave circuit which is essentially equivalent in design and function to the medium-wave circuit with the varicap-diode BB 113, already described in Design Examples of Semiconductor circuits, edition 1974. The r.f. circuit L_2 consists of a single-layer cylindrical coil (without any screening can) and is connected to two systems of the BB 113 via a shortening capacitor of 220 pF. Only by this capacitor it was possible nearly to achieve a constant Q unloaded of about 100 over the total frequency range. The control voltage is supplied to the varicap-diode via a 100-kΩ-resistor being in parallel to the shortening capacitor. The antenna coil and the decoupling turns for the mixer transistor BF 324 are connected to the tuned circuit by a weak coupling to attain better selectivity.

The conversion gain of the BF324 is intentionally kept down to a value of 10 to 12 db. Thereby the selectivity and the behaviour of large input signals received from strong stations are improved, but the gain is high enough to maintain a sufficient signal-to-noise ratio. Optimum conditions are given with an emitter current of about 7 mA and an oscillator voltage of 350 mV_{pp} at the base of the BF324. The function of the diode D_1 (BA182) should be briefly explained, too.

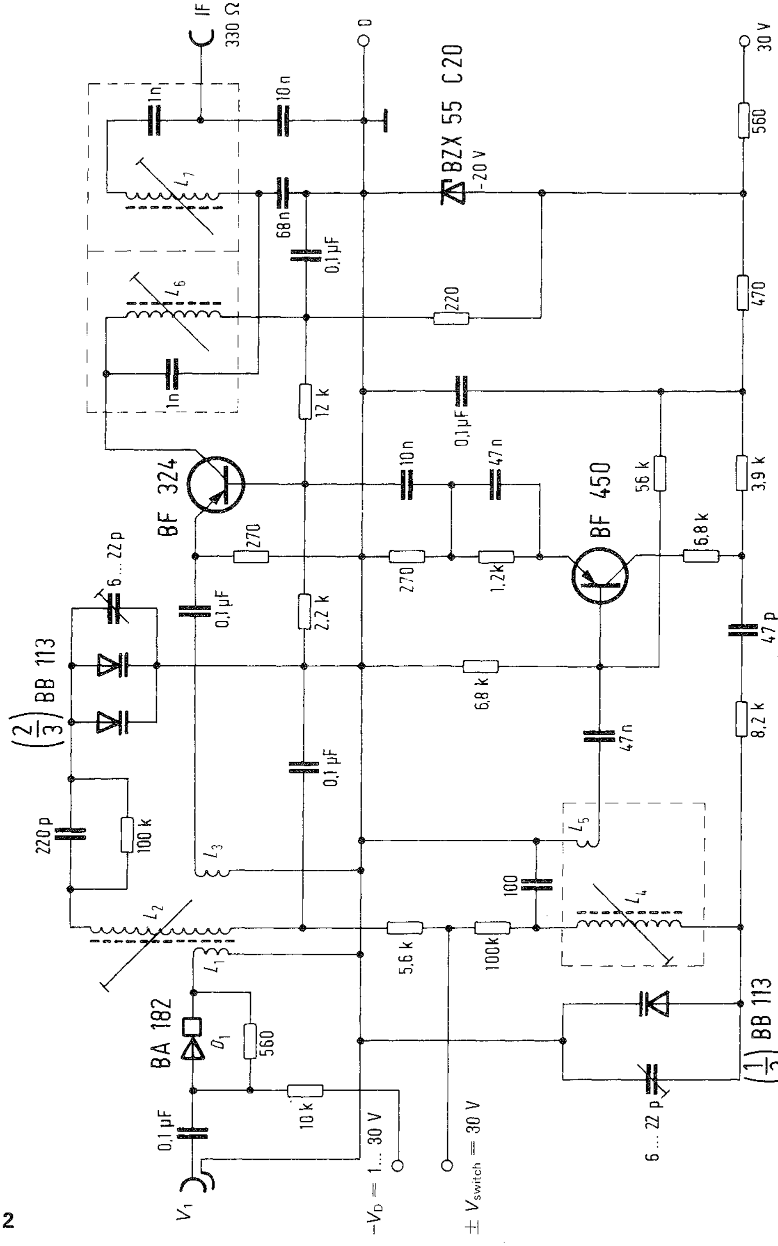


Fig. 1.2

It is conductive if the signal received from a transmitting station is low. At high signal levels, however, the diode is reverse biased by the IF-control voltage (reversing of the switching voltage). By this measure the antenna signal is stepped down by a voltage divider consisting of the 560 Ω-resistor and the transformed input impedance at L_2. Thus the permissible r.f.-levels at the antenna input are in order of some V_{pp}. The oscillator is tuned by the third system of the BB 113. The 100 pF-capacitor, required for the tuning range as well as for the tracking, takes positive effect to the stability of the tuning voltage due to the fact that the characteristic curve of the BB 113 becomes less steep. In addition to that higher input signal levels are permissible at low frequencies, because of the capacitive division at the high-impedance end of the circuit. The oscillator transistor is run with grounded emitter connection and is overdriven in the way that a voltage with a limited, nearly rectangled amplitude is available at its collector. At the tuned circuit, however, the amplitude is sinusoidal, since it is weakly coupled to the collector by a RC-circuit. The oscillator voltage for the mixer is coupled out at the non-bridged part of the emitter resistor and a sinusoidal oscillation with nearly constant amplitude and low internal impedance is achieved (inverse feedback for the mixer).

The frequency range of 5.8 to 10.5 MHz includes the 49-m-band (6 to 6.2 MHz), the 41-m-band (7.2 to 7.3 MHz) and the 31-m-band (9.5 to 9.7 MHz).

Due to the wide tuning range it is recomended to use an electronic magnifier with an additional potentiometer of, e.g., 500 Ω, connected to the tuning potentiometer of 50 kΩ (at the upper end)

The table below indicates the results of a test with a sample board.

f_{in} MHz	R_{in} Ω	G_p db	V_{in} max (m=30%) for k_{AF}=10% mV_{pp}		V_{osc} mV_{pp} (base mixer)	$-V_{tuning}$ V	$-V_{tuning}$ for Δf_{osc} = 1 kHz mV	stability of tuning voltage refered to 30 V in ‰
			D_1 conductive	D_1 non conductive				
6	45	10	170	3700	300	1.54	5.1	3.3
8	67	11.1	170	4400	350	12.58	9.4	0.75
10	85	12.3	160	2500	300	22.76	29.2	1.28

Technical data:

Supply voltage	V_S = 30 V
Total supply current	I_{tot} = 20 mA
Tuning voltage	V_{tun} = 0.5 to 30 V
Switching voltage for BA 182	V_{switch} = ±30 V

Coil data:

L_1 = antenna coupling 60 Ω
8 turns, CuL, 0.12 m ⌀
L_1/L_2-distance = 5 mm
L_2 = r.f.-circuit, 26 turns, 12×0.05 Cu LS
L_2/L_3-distance = 3 mm
L_3 = r.f.-coupling, 2 turns, CuL, 0.25 mm ⌀

Coil formers:

⌀ 5 mm, core 20 K 12, 10 to 20 mm long
L_4 = oscillator circuit, 25 turns, 15×0.05 Cu LS
L_5 = oscillator feedback, 5 turns, Cu L, 0.12 mm ⌀
1×Vogt filter kit D 41-2520
L_7 = 1st. band-pass circuit, 85 turns, 12×0.04 Cu LS
L_8 = 2nd band-pass circuit, 85 turns, 12×0.04 Cu LS
2× Vogt filter kit D 41-2519

1.3 Antenna-amplifier with BFT 12 for FM-range

The only way to improve the reception of FM-signals or particularly of stereo FM-signals under disadvantageous receiving conditions is to amplify the antenna signal. This should be made directly at the antenna, since the loss is increased meter by meter of any cable. In most cases higher line attenuations can be expected than usually calculated. Even receivers with an additional noise figure of zero do not show any improvements of the signal-to-noise ratio becomes too low because of a long transmission line. Therefore it is practically useless to require extremely low noise figures only for the receivers.

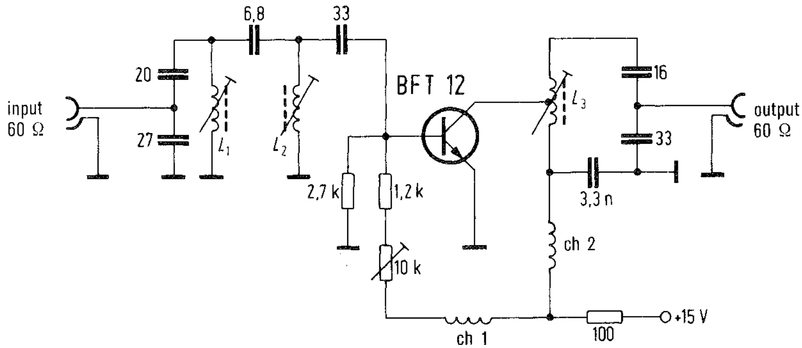


Fig. 1.3

To avoid interferences of signals received from stations of other bands it is propitious to amplify the FM-band only. The band amplifier shown in **Fig. 1.3** is connected directly to the 60-Ω-output of the FM-antenna, i.e. it is placed at the top of the antenna pole. The matching is achieved by the input band-pass connected to the base of transistor BFT12, being a typically linear silicon transistor for broadband amplifiers. The output filter matched accordingly to a 60-Ω-coaxial line is connected to the collector. The operating voltage of 15 V can be supplied by the coaxial line.

Technical data:

Power gain G_p = 22 db
Noise figure F = 3.5–4.0 db or 2.2–2.5 KT_o
Input and output reflexion coefficient $|r_i|$ and $|r_o| \leqq 0.3$
$d_{im\ (60\ db)}$ at V_{out} = 680 mV
$d_{im\ (50\ db)}$ at V_{out} = 1000 mV

Optimum operating point of minimum intermodulation
$I_C \approx 80$ mA $\quad V_{CE} \approx 7$–7.5 V
Supply voltage 15 V

Coil data:

Vogt coil former, ordering code: Sp 3.5/16.6–2048 C
Core: U 17
L_1: 5 turns Cu 0.6 mm ⌀
L_2: 3 turns Cu 0.6 mm ⌀
L_3: 3+2 turns Cu 0.6 mm ⌀
Choke Ch_1 = Ch_2: 20 turns Cu L 0.3 mm ⌀, cross section of winding = 4 mm

1.4 Three-stage broadband antenna amplifier with BFT 12

Fig. 1.4 shows a design example of a three-stage broadband amplifier using the latest UHF-broadband-transistor BFT12, offering a high gain. Intermodulation and noise figure conclude from the wide dynamic range of this output-stage transistor, which is linear already at power dissipations of 0.5 W. The special T-plastic-case meets all requirements according to r.f.-parameters, heat abstraction and economy. With the sample board a thermal resistance of R_{th} = 120 K/W is achieved. With respect to the special measures taken to guarantee a high reliability this transistor BFT12 applies also to all requirements of professional circuits.

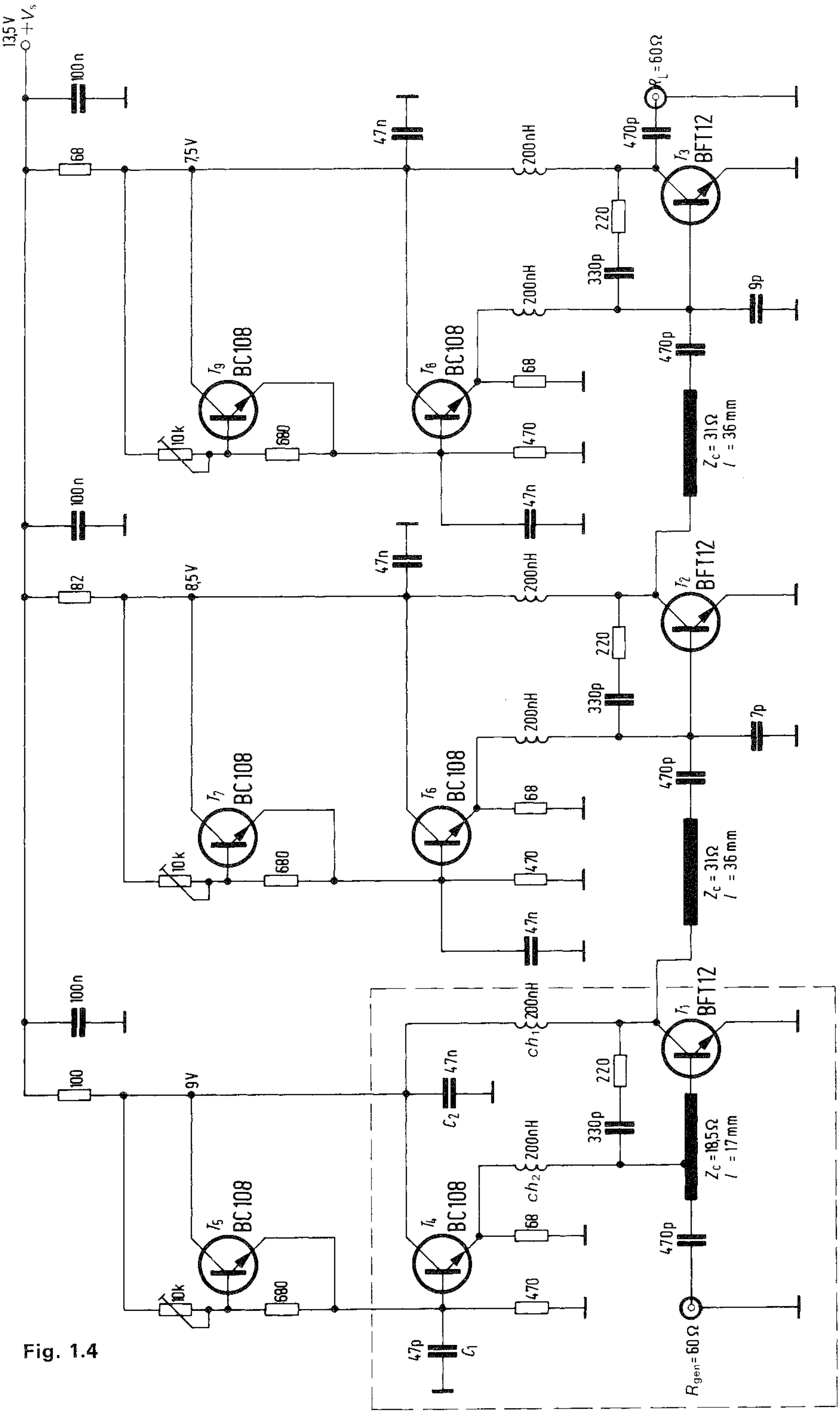
All three stages of the broadband amplifier are equipped with the BFT12 and are similar in design on principle. The circuit consisting of transistor T_4 and T_5 controls the operating point of the first stage with T_1. The base of transistor T_1 is connected to the emitter of the common-emitter circuit T_4 via the choke ch_1. The source impedance of the common-emitter circuit is 3 to 4 Ω. The combination of the capacitor C_2 and the choke ch_2 connected to the emitter of T_1 has the response of a low-pass filter with a low impedance for the video-frequency range. Both measures reduce the beginning of unwanted mixing frequencies, increase the obtainable output voltage V_{out} with reference to a given intermodulation distance and improve the dynamic range of the amplifier.

If a composition of different signals is amplified, non-linear components (e.g. transistors) will generate interferences like cross modulation and intermodulation. In general these interferences are derived from the third-power part of a mathematical series expansion for the transfer characteristic. However, it has been experienced that interferences created by the part of second power are superimposed to the above mentioned ones. Interferences appear at common-emitter circuits. They are generated the base and collector by the second-power part of the characteristic and they can be reduced by low-ohmic impedances in the total video range. Thus the modulation of signals by these interferences is diminished and the cross modulation as well as the intermodulation behaviour is improved.

At relatively low power dissipation, but high power gain and linearity, the new r.f. broadband transistor BFT12 can be used without any problems. Besides that if offers an optimum economy.

Electrical characteristics of the UHF-broadband-amplifier

Supply voltage	V_S = 13.5 V
Supply current	I = 205 mA
Number of amplifier stages	n = 3
Frequency range	20 to 860 MHz
Power gain (at R_g = R_L = 60 Ω and f = 800 MHz)	G_p = 24 db
Noise figure (at R_g = R_L = 60 Ω and f = 800 MHz)	F = 7.5 db
Output voltage (at R_g = R_L = 60 Ω and f = 800 MHz, d_{im} = 60 db, according to method of two transmitters)	V_{out} = 400 mV



13,5 V
+Vs
100n
68
7,5 V
47n
200nH
470p
RL = 60Ω
BFT12
T3
220
330p
9p
BC108
T9
T8
10k
680
470
Zc = 31Ω
l = 36 mm
82
8,5 V
BFT12
T2
7p
T7
T6
BFT12
T1
100
9V
C2
ch1
ch2
Zc = 18,5Ω
l = 17 mm
T5
T4
47p
C1
Rgen = 60 Ω

Fig. 1.4

1.5 Two-stage broadband amplifier from 1 to 1000 MHz using BFT 65

The excellent high frequency characteristics of the UHF-silicon-transistor BFT65 as low-distortion, low noise figure and high stage gain are demonstrated by the following application example of a two-stage broadband amplifier **(fig. 1.5)**.

The broadband amplifier consisting of two BFT65 is mounted on a copper-faced pc board with the dimensions of 50×50 mm. In the frequency range of 1 to 1000 MHz a gain of 20 db is attained at a noise figure of 5 db. The output voltage is 130 mV at an intermodulation loss of 60 db. The first transistor T_1 operates with a collector current of 8 mA and the second one with 20 mA.

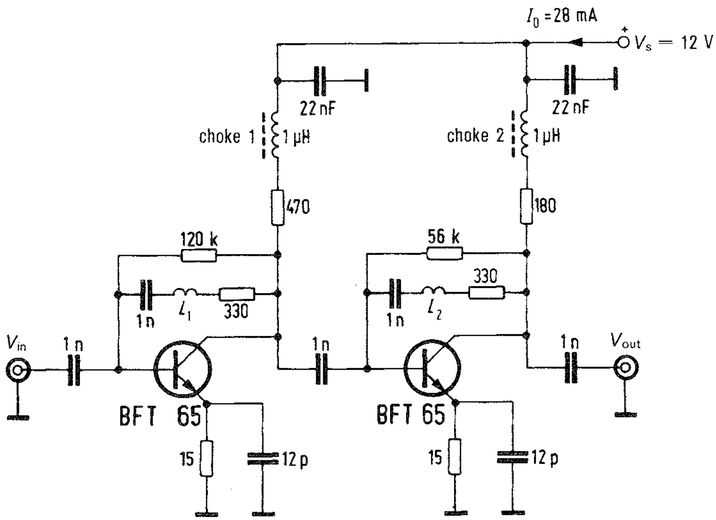


Fig. 1.5

The broadband gain response is achieved by the emitter resistor of 15 Ω.

To avoid an additional decrease of gain by inverse feedback of the emitter inductance in the upper frequency range, the inverse feedback combination consisting of 15 Ω ‖ 12 pF must have a low inductance. Therefore the emitter capacitors are proportioned so that the increasing influence of the emitter inductance is compensated at frequencies higher than 500 MHz.

The impedance matching of the input and output of each stage is achieved by a parallel feedback resistor of 300 Ω. The inductances L_1 and L_2 compensate the phase response of the resulting feedback in the frequency range > 600 MHz in such a manner that the impedances are matched even if the input conductances of the transistors increase.

Characteristics

Supply voltage	V_S = 12 V
Supply current	I_S = about 28 mA
Power gain (1 to 1000 MHz, $R_g = R_L = 60\ \Omega$)	G_p > 20 db
Noise figure (1 to 1000 MHz, $R_g = R_L = 60\ \Omega$)	F < 5 db

Standing wave ratio (1 to 1000 MHz, $R_g = R_L = 60\ \Omega$) $S < 2$

Output voltage ($f = 800$ MHz, $R_g = R_L = 60\ \Omega$) $V_{out} = 130$ mV

Attenuation of intermodulation $d_{im} > 60$ db

T_1, T_2	BFT 65
Ch_1, Ch_2	Choke, 2 turns, CuL 0.25 mm ∅, on double aperture core, B62152-A0007-X001
L_1, L_2	the terminal wires of resistors R_2, R_6 are wound to coils with about three turns having a cross section of 25 mm ∅
1 nF	30 V disc capacitor
22 nF	30 V disc capacitor
12 pF	trapezoidal disc capacitor
15 Ω	low-inductance resistor (metal film)

1.6 Three-stage broadband amplifier for a frequency range of 30 to 900 MHz with BFR 34 and BFS 55

The ability of modern silicon r.f.-transistors is demonstrated in the following application of a broadband amplifier using a standard circuit.

The following electrical data were achieved:

Gain	32 db
Noise figure	5 db
Output voltage	105 mV
$d_{IM\ II}$	60 db

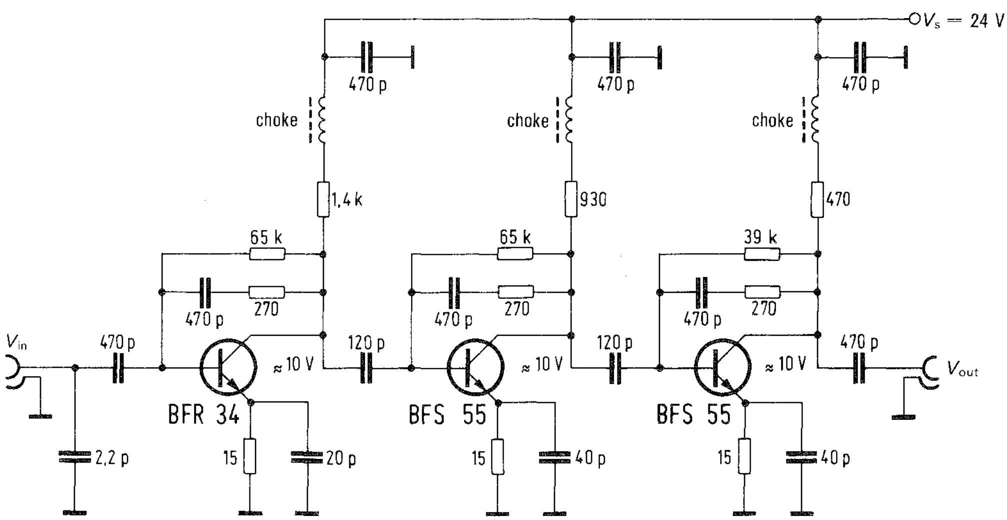


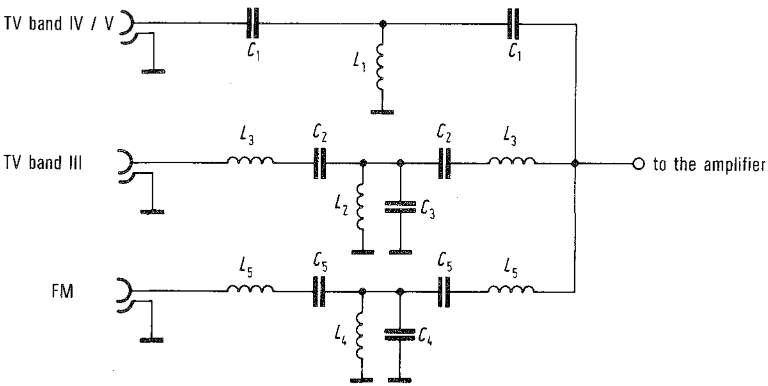
Fig. 1.6

The amplifier is mounted on a pc board (glassfiber reinforced epoxy) with the dimensions of 60×80 mm and uses the transistors BFR 34 and 2× BFS 55. The supply voltage is 24 V. The amplifier consists of RC-coupled common-emitter circuits and has a negative feedback. The series and parallel feedback circuit has to perform two functions.

a) nearly to linearize the gain response over the frequency range and
b) to match the input and output impedances of the amplifier to the ones of the signal source respectively of the load.

The circuit is dimensioned in such a manner that its influence is reduced at higher frequencies. The transistor BFR 34 operates at $V_{CE} = 5$ V and $I_C = 10$ mA.

The average gain is about 32 db, whereat the one of the prestage is about 11 db. A noise figure of < 5 db is achieved at a frequency $f = 800$ MHz. Another performance of the BFR 34 is that the basic noise is independent of the current. Particularly at large signal operation this feature is of noticeable advantage, since the maximum distortions take place in the range of higher collector currents. An output voltage of 105 mV is attainable for the three-stage amplifier at 800 MHz and at an intermodulation loss of 60 db (simulated SSB test method). Additional frequency separating networks obtain the decoupling of the inputs required for antenna amplifiers with different ranges. The network shown in **fig. 1.6.1** is dimensioned for the FM-range, the TV-band III and the TV-band IV/V.



$C_1 = 3.3$ pF $\quad L_1 = 3$ turns
$C_2 = 8.2$ pF $\quad L_2 = 4$ turns
$C_3 = 22$ pF $\quad L_3 = 8.5$ turns $\quad$ core ⌀ 2.5 mm, 0.7 mm ⌀ CuL
$C_4 = 90$ pF $\quad L_4 = 12$ turns
$C_5 = 47$ pF $\quad L_5 = 13$ turns

Fig. 1.6.1

1.7 Interference-immune FM- tuner

The following FM-tuner shown in **fig. 1.7** has been designed with special respect to interference immunity, narrow bandwidth, sufficiently low noise factor and good oscillator stability.

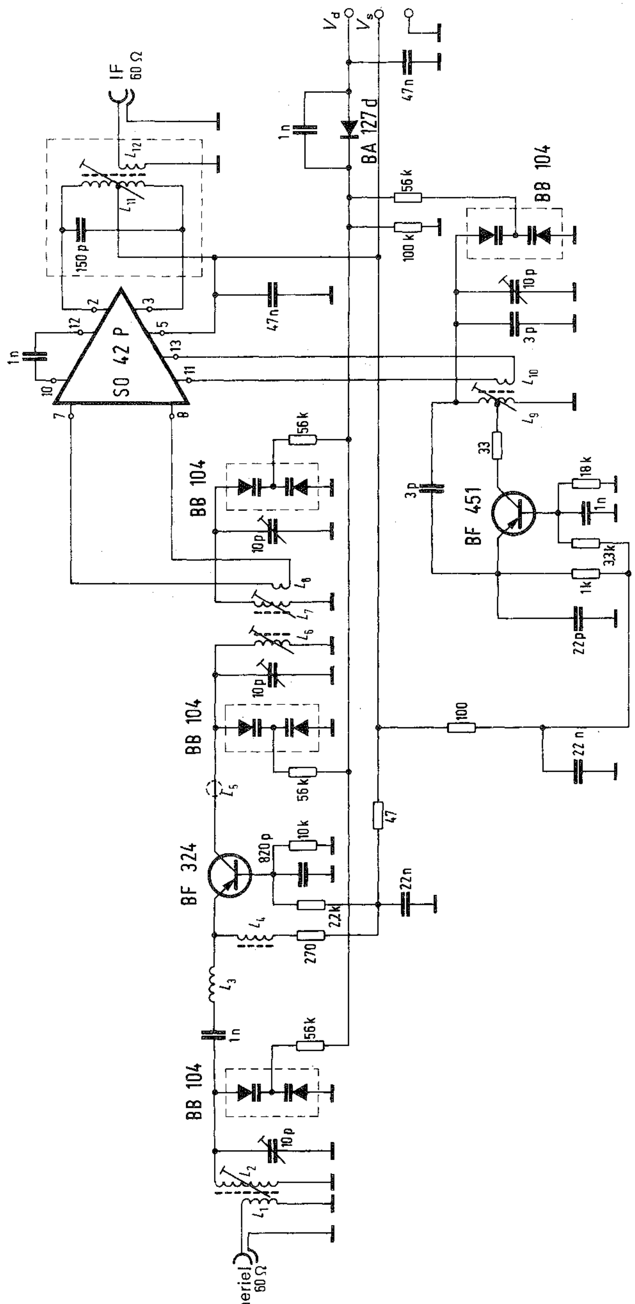


Fig. 1.7

The RF-input circuit is tuned by the double-capacitance diode BB 104, being in push-pull operation. With special respect to optimum noise figure it is matched to the pre-stage transistor BF 324 by L_3. The bandwidth of the r.f.-band-pass is adjusted in the way that the total noise figure does not exceed 5 db. The operating point chosen for the BF 324 achieves a good interference immunity at a sufficiently low noise figure of the transistor. Possible UHF-oscillations of the front end are suppressed by a ferrite bead and an accurate grounding of the base.

The ring mixer S 042 P can be coupled very weakly to the r.f.-band-pass filter due to its extremely low noise figure. Thus a very good selectivity of the mixing stage is achieved. Besides that the level at the mixer input is kept low, whereby the generation of interference mixing products is reduced.

A 33-Ω-resistor is connected to the collector of the oscillator transistor BF 451. Thus UHF-oscillations are prevented and the content of harmonics is minimized.

On account of the symmetrical wiring of the S 042 P and the separating stages with transistors operating at impressed currents the feedback of the RF-input signal to the oscillator is negligible. The oscillator frequency-detuning is less than 10 kHz at RF-input signals up to 3 V.

Characteristics

Supply voltage	12 V
Supply current	9.5 mA
Tuning voltage	4 to 25 V
Input impedance	60 Ω
Output impedance	60 Ω
Power gain	27 db
RF-bandwidth	1.1 to 1.2 MHz
IF-bandwidth	400 kHz
Noise figure	5 db
Temperature drift of oscillator	< 1.5 kHz/K
Oscillator frequency-detuning over RF-input voltage	< 10 kHz to V_{in} = 3 V

Coil data:

L_1	2 turns	0.5 mm ∅ CuL	
L_2	6 turns	0.8 mm ∅ CuAg	
L_3	12 turns	0.2 mm ∅ CuL	
L_4	18 turns	0.2 mm ∅ CuL	
L_5	ferrite bead	B62110 K12 3.5×1.6×6	
L_6	5 turns	0.8 mm ∅ CuAg	
L_7	5 turns	0.8 mm ∅ CuAg	
L_8	2 turns	0.5 mm ∅ CuL	
L_9	7 turns tap at 5.5 turns	0.8 mm ∅ CuAg	
L_{10}	2 turns	0.5 mm ∅ CuL	
$L_{1, 2, 6, 7, 8, 9, 10}$		on coil former 4.3 mm ∅	
$L_{1, 2, 6, 7, 8}$		threaded core B63310-B3021-x017	
$L_{9, 10}$		threaded core 3.5×0.5×10 of brass	
L_3		on Vogt coil former Sp 4/9 – 2053 A	
L_4		cylinder core B61110 U17 2×6	
L_{11}		6 turns ea.	0.2 mm ∅ CuL
L_{12}		2 turns	0.2 mm ∅ CuL
$L_{11, 12}$		on Vogt filter kit D 41-2520	

1,8 4-GHz-oscillator with BFR 34 A

The mechanical construction of a 4-GHz-oscillator, designed with the transistor BFR 34 A, is shown in **fig. 1.8.**

An output power of 12 mW ist achievable at an operating point of V_{CE} = 12 V and I_C = 17 mA.

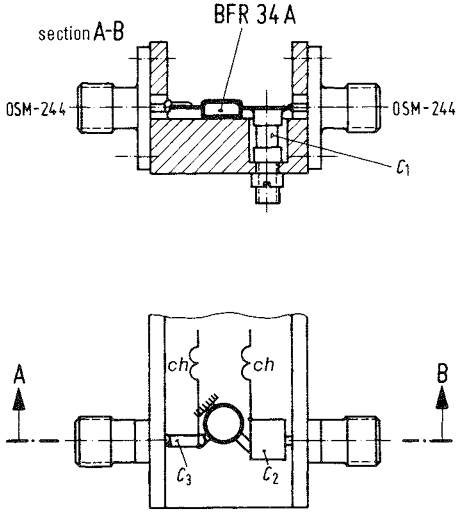


Fig. 1.8

The oscillator operates as a common-base circuit. The collector is connected to ground in order to improve the cooling of the transistor chip mounted in a plastic case. The optimum phase condition of the feedback between emitter and collector is adjusted by a coaxial line-stretcher. The coupling capacitor C_2 to the output is formed by a metal plate with the dimensions of about 5×5 mm.

The d.c. is supplied via lead-through filters and chokes using ferrite beads (1 turn).

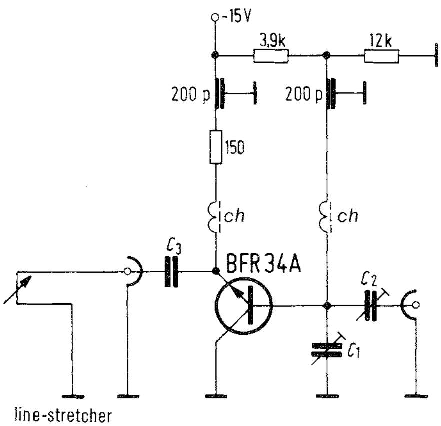


Fig. 1.8.1

The resonant circuit which actually determines the frequency include the collector capacity of the transistor and the inductors of the surrounding circuit. At 4 GHz the inductance of this resonant circuit has to be very low and has to present a high Q. Besides that a good separation between base and collector terminal has to be enabled. This requirement can be realized by an air trimmer capacitor (C_1) with low inductance and high Q. If this capacitor is operated at series resonant frequency, it takes the effect of a variable inductor. Its series inductance is reduced in addition, if the trimmer is placed in a bore-hole.

The maximum of the output power and of the transition frequency f_T is attained at a current in the range of 15 to 20 mA. At $V = 12$ V an average value of 12 mV into 50 Ω has been measured for the max. output power.

By a test with a spectrum analizer it had been demonstrated that the difference between the spectral line of the oscillator frequency and the noise was greater than 50 db; the difference to the first harmonic at 8 GHz was 30 db.

The BFR 34 A is suitable as r.f. pre-stage transistor offering low noise figure and as oscillator transistor up to 4 GHz. According to the available r.f.-power this transistor is favoured for a variety of applications: general test purposes, microwave generator for short-range radar, diode mixers, and parametric converters or amplifiers).

1.9 UHF-tuner using the high-current transistor AF 379 in prestage and mixer

With increasing numbers of broadcasting stations TV-tuners have to be able to handle higher r.f.-input signals more than in the past, especially if they are used in colour TV-sets. The developement of the UHF high-current-transistor AF 379 and the PIN-diode BA 379 turned out to be one of the solutions to this problem. Due to the wide dynamic range of the AF 379 and the high signal level handling capability of the BA 379 a considerable improvement of the cross modulation behaviour has been obtained.

Interferences generated by too high antenna signal levels occures especially in the front end, as the following two-circuit bandpass filter prevents the mixer from r.f.-input signals with wider frequency spacing. For this reason the transistor AF 379 is used only in the front end. With increasing numbers of transmitting stations it happens that the spacing between the signals received is only 2 or 3 chanels.

In this case the selection of the intermediate band-pass filter is no longer sufficient to suppress satisfactorily the antenna signal, amplified by the pre-stage. Therefore the cross-modulation immunity of this frequency range is determined by the mixer stage and it is essentially lower than for other frequencies being far away.

Thus it is necessary to improve the large signal characteristics also of the mixer. This can be obtained by replacing the usual mixer transistor by the high-current transistor AF 379 with its excellent capability to handle high signal levels. As this feature of the AF 379 takes an effect only at current higher than 4 mA the mixer has to be driven by a separated oscillator stage.

According to the different requirements the mixer and the oscillator can be dimensioned distinctly, so that the increased number of components is in relation to the adequate improvement of quality.

With a sample tuner the following results had been experienced in the frequency range of 470 to 800 MHz. The circuit is shown in **fig. 1.9.**

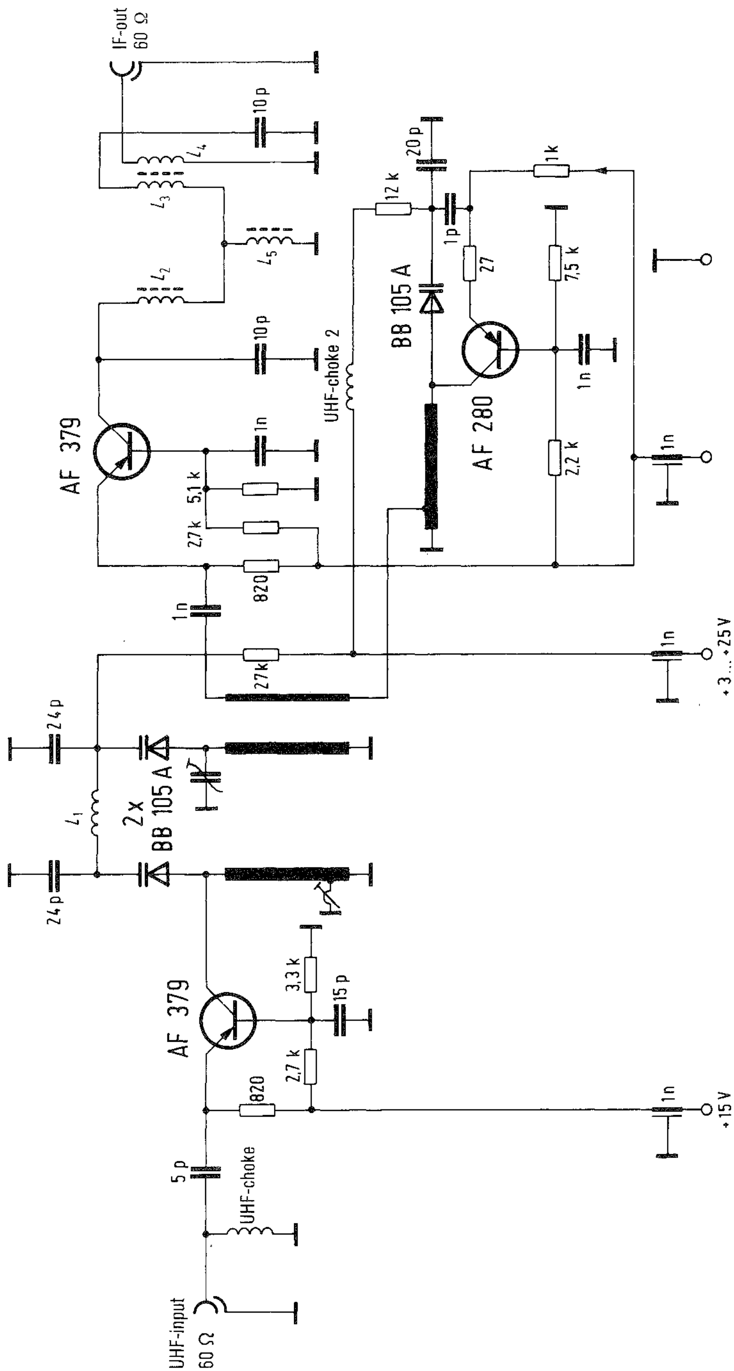

IF-out
60 Ω
10 p
L_4
L_3
L_5
L_2
20 p
12 k
1k
1p
27
7,5 k
BB 105 A
UHF-choke 2
AF 280
1n
2,2 k
AF 379
5,1 k
27k
820
+3 ... +25 V
24 p
2x
BB 105 A
L_1
3,3 k
15 p
2,7 k
+15 V
5 p
UHF-choke
UHF-input
60 Ω

Fig. 1.9

Power gain	G_p = 18 to 23 db
Noise figure	F = 6–7.2 db
Input reflexion	r = 0.4 to 0.7
UHF bandwidth	B = 15 to 22 MHz
IF-band-pass filter	B_{IF} = 10.5 MHz
IF-band-pass filter ripple	w = 1 db
Image rejection	a_{im} > 40 db

If the signal-to-image ratio is to be improved, e.g., to a value of greater than 60 db, then only two solutions are practicable, either an additional pre-stage is connected infront of the first transistor, or the IF is shifted into a range which is higher than that of band 1.

As the cross-modulation immunity is especially of interest, fig. 1.9 1 shows the curves of cross modulation for adjacent channels at effective frequencies of 500 MHz and 790 MHz (tuner no. 3). In comparison there are also shown the test results of two other tuners with different but commonly used circuit-concepts. The effective frequency is 650 MHz.

Tuner no. 1: Using high-current prestage transistor AF 379, broadband UHF-input and self-oscillating mixer,

Tuner no. 2: Selective input band-pass filter, silicon-UHF-prestage-transistor and diode-mixer

Tuner no. 3: Three-transistor-concept with high-current mixer and high-current prestage as described above.

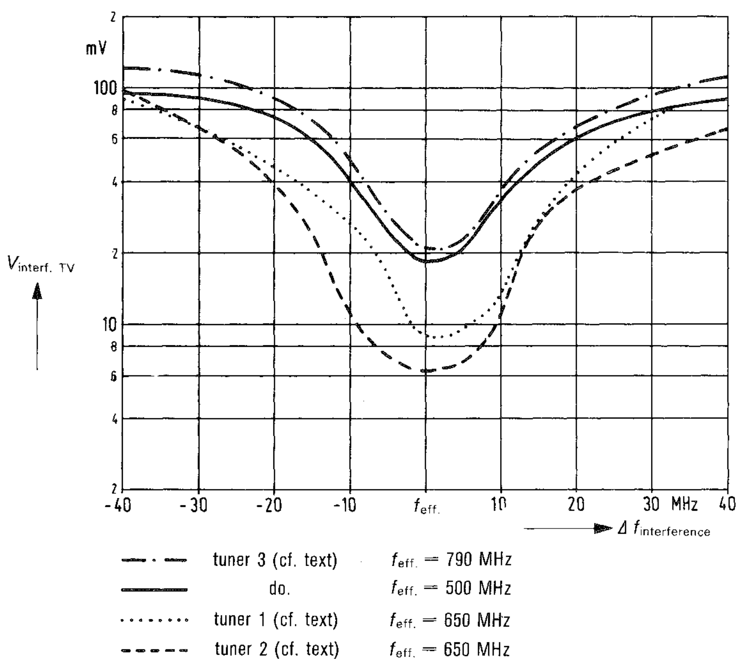


Fig. 1.9.1

Coil data:

L_1:	8	turns	0.42 CuLL	Air coil 3 mm ⌀
L_2:	12	turns	0.32 CuLL	Coil former 4.3 mm ⌀
L_3:	14	turns	0.32 CuLL	Siferrit-core U17*)
L_4:	3	turns	0.32 CuLL	10 mm long, 3.5 mm ⌀
L_5:	6.5	turns	0.42 CuLL	wound on Siferrit-core*)

*) Ordering code: B63310-B3021-X017

1.10 FM-tuning indicator with light emitting diodes

For FM-IF-amplifiers using the limiting and demodulating IC TBA 120 a zero-axis-crossing indicator with three light emitting diodes has been designed (cf. **fig. 1.10**).

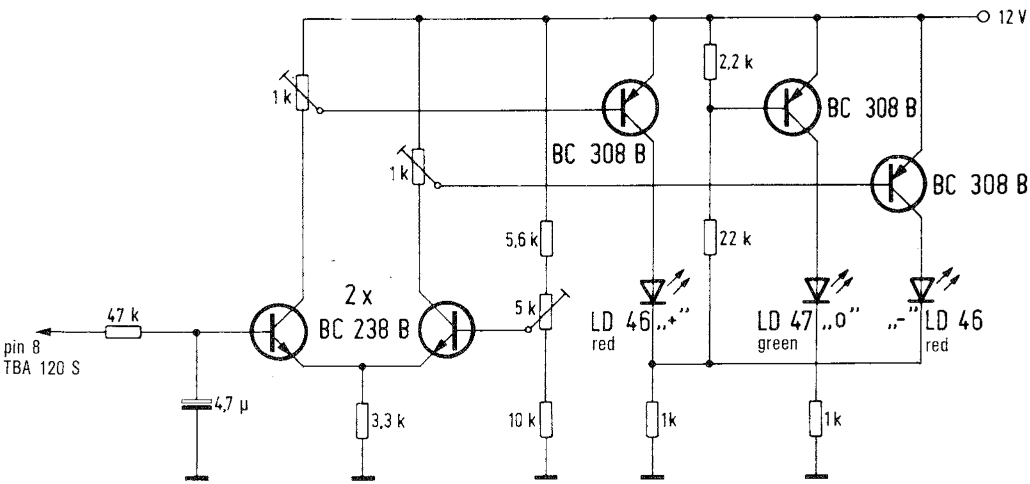


Fig. 1.10

The output voltage available at pin 8 of the TBA 120 is integrated by a RC-circuit and amplified by a differential amplifier. If a detuning occurs with reference to higher frequencies the output level of the TBA 120 increases, i.e. the left transistor (BC 238 B) of the differential amplifier is turned on, the BC 308 B becomes conductive and switches on the red "+"-LED, type LD 46. With regard to lower frequencies the "−"-diode is turned on. In both cases there exists a voltage drop at the cathode resistor being common for both red LEDs and the switching transistor for the green LED is turned off. On account of this NAND-operation the "0"-diode emits light only if none of the red diodes is switched on.

The differential amplifier is symmetrically adjusted by the 5-kΩ-potentiometer at nominal value of the IF. The threshold of the red light emitting diodes is adjusted by the 1-kΩ-potentiometer.

2. Circuits for monochrome TV-receivers

2.1 Pulse separation and phase comparison

The following circuit shown in **fig. 2.1** effects the pulse separation of negatively directed line pulses from the video signal, comming preferably from the video preamplifier. This video signal should be about 1 to 4 V_{pp}. It is supplied via the capacitor C_1 and the resistor R_{13} (if needed) to the base of transistor T_1 negatively biased by resistor R_{12}. When the signal is missing nearly the total positive supply voltage is applied to the capacitor C_7 via the switched-through transistor T_1 and the conductive diode D_3. Thus the h-generator oscillates at nominal frequency f_0.

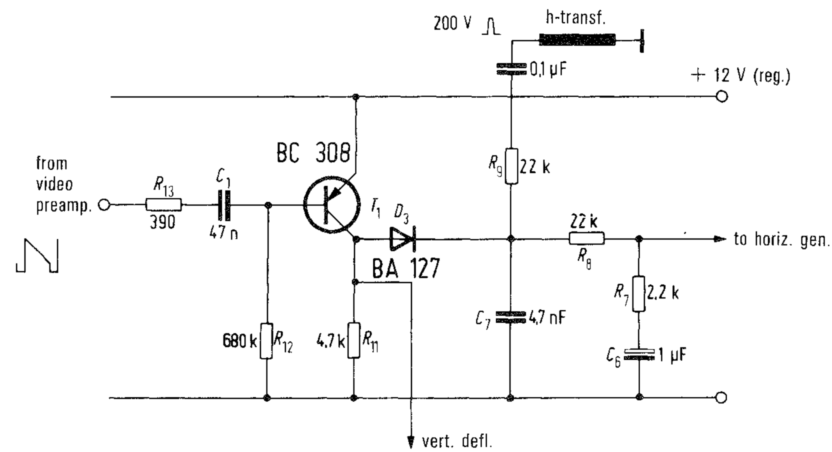


Fig. 2.1

If there is a video signal, a positive bias voltage arise at C_1 as a result of the (greater) negative synchronizing pulses. This voltage shifts the video signal into the cutoff region, so that only the negative synchronizing pulses drive (in this case very hard) the transistor. Negative pulses with an amplitude of 12 V and a duration of about 4 µs are available at the collector.

A reference pulse comming from the horizontal transformer via R_9 is integrated at the capacitor C_7, resulting in a saw-tooth voltage, which is superimposed upon the supply voltage of 12 V (cf. **fig. 2.1.1**). The synchronizing pulse passes the transistor T_1 and at a given moment (phase comparison) the delta voltage is added to the supply voltage (less residual voltage of T_1 and D_3). Thus it is possible to shift the delta voltage up and down, whereby the average value, both as positive and negative voltage, is added to the 12 V. Resistor R_7, in combination with R_8 and C_6, realizes the filtering in the direction of the horiz.-generator. Capacitor C_6 integrates rapid voltage changes which can be caused by interference pulses, so that the horizontal generator can maintain its frequency very constantly.

It is recommended to pick up the comparison pulse of 200 V_{pp} at the collector of the line transistor by adding a coupling capacitor (e.g. 0.1 µF). By this measure it is achieved that the picture phase position is only slightly affected by reactions of the sound circuit and of the power supply voltage (30 V), caused by load changes, especially by those of the beam current. In any case a stabilization of the 12-V-supply voltage is necessary.

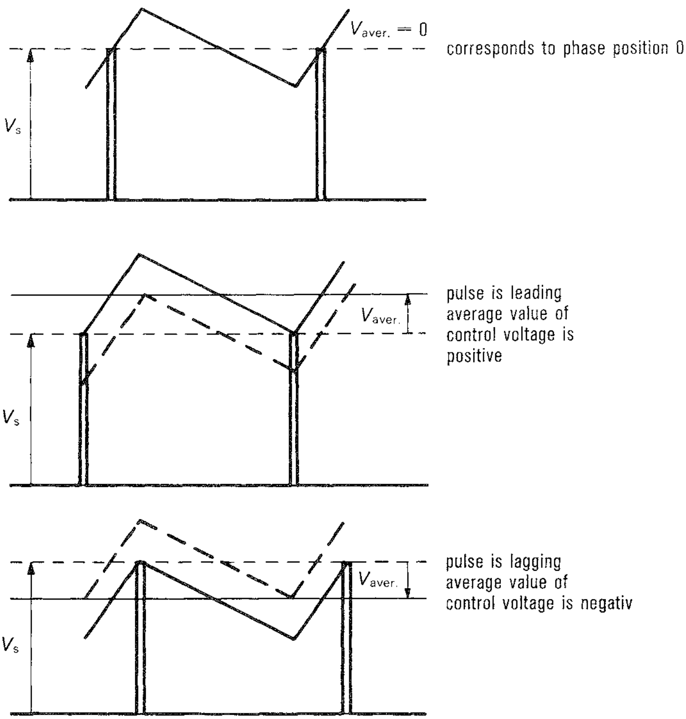


Fig. 2.1.1

2.2 Pulse separation, horizontal generator and driver

The combination of a horizontal generator and a driver, described in the following and shown in **fig. 2.2**, is a very simple and economical solution. Pulses with a duty factor of about 1 : 2 are supplied from the driver transistor BD 137 (BD 139) to the base of the line switching-transistor via the transformer Tr. Thereby it is possible to set the desired minimum value of the base current by choice of the operating voltage and possibly of the base resistance of R_1. The protection circuit K_{13}/C_9 clips the narrow fly-back pulse caused by the stray inductance of the transformer. After that the transformer supplies its energy to the line output stage, i.e., when the transistor BD 137 is still reversed. The reverse time is determined by the circuit of C_4/R_3.

The conducting time is influenced by the circuit C_3/R_6 and adjustable by the control voltage or the resistor R_6. Thereby also the reverse time is changed in the same way, that the duty factor will not vary. The z-diode has a very important function. It achieves that the frequency f_o is built up to its nominal value at about ½ to $^1/_3$ of the supply voltage. This is important for fear that the line output stage operates probably at too low frequencies, causing inadmissibly high fly-back voltages. The clamping diodes D_1/D_2 protect the capacitor C_3 from a higher voltage than 12 V. Thus the time lapse of the drivers reverse period depends only on C_3/R_6 and not on the fly-back voltage level at the collector of the transistor BD 137.

Tr. EE 20 (B78002-A205-F1)
Airgap: L ≈ 0.3 mm (total)
Mat.: Siferrit T 26
B66205-A0000-R026
Coil: B66206-A1001-M001
Fixing clip: B66206-A2001-X000
or glue the core

2– 4	150 turns	0.20 CuL	(inside)
9–10	30 turns	0.35 CuL	(inside)
6– 8	150 turns	0.20 CuL	(outside)

● same polarity

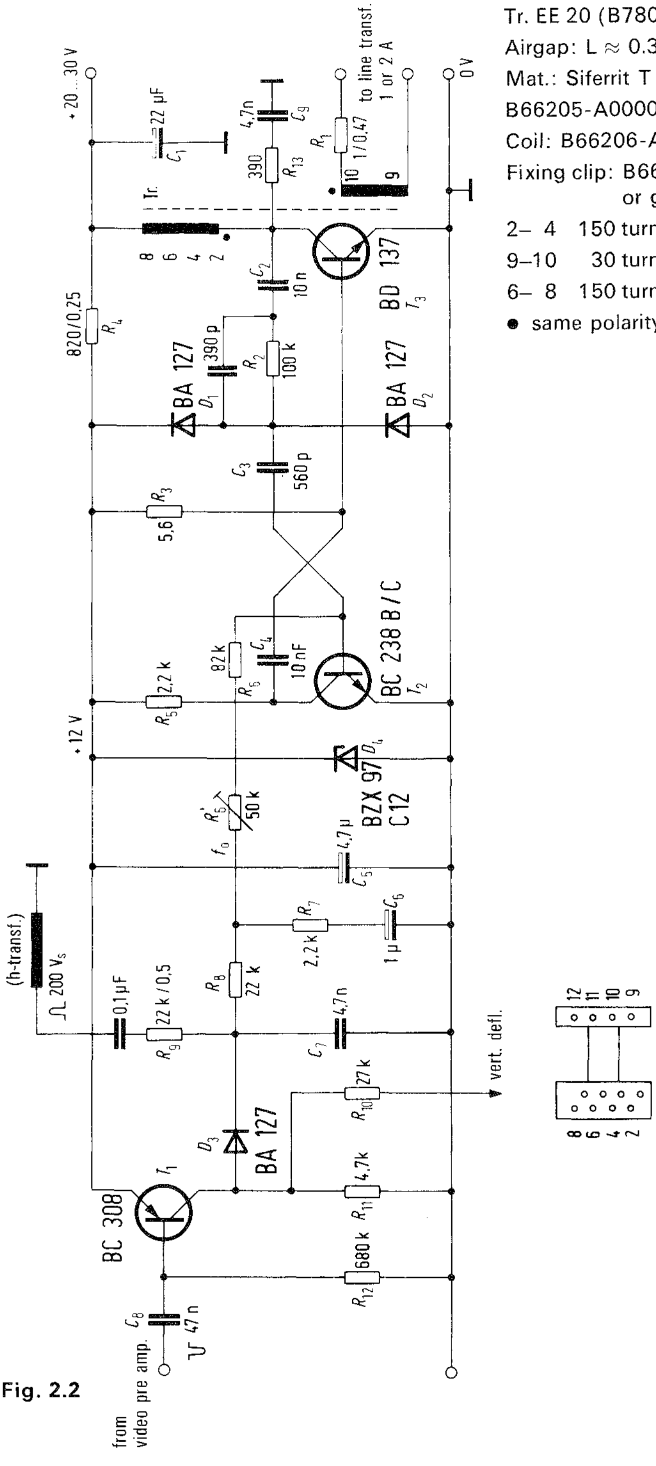


Fig. 2.2

Another advantage of this generator is the fact that it starts immediately to oscillate. After connecting the supply voltage to the unit the base of the line output stage transistor is driven hardly within a few seconds and the maximum values can be reached after 2 to 3 ms. This is also very important, since the use of synchronization power supplies require a strong synchronization which is immediately obtained. Oscillation starts of other frequencies are only possible in the same area of characteristics, i.e. at low currents and low voltages.

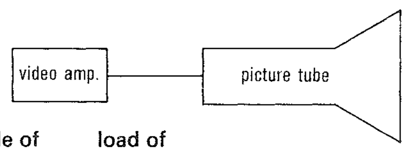
The transformer EE 20 can be varied in seize and shape, whereby C_9 and R_{13} have also to be changed. Essentially the transformer has to be able to store sufficient energy, otherwise the circuit R_3/C_5 does not determine the forward and back stroke.

V_S	I_B for R_B		$1/f$
V	0.67 Ω	1 Ω	µs
30	1.8	1.3	64
25	1.6	1.1	68
20	1.25	0.8	70
15	0.8	0.6	73
10	0.5	0.4	90
5	–	0.1	106

It can be learned from the table how the generator reacts at the beginning of oscillations (f). Besides that it can also be infered which operating voltage has to be chosen for the driver and which value has to be used for the base resistor R_1 of the line output stage.

The driver transistor of this horiz. generator is driven in push-pull operation with reference to the line output stage (not drawn in the schematic).

In order to complete the horizontal generator the pulse separation and the phase comparison circuit (cf. **fig. 2.1**) have been combined to the schematic diagram shown in **fig. 2.2.**



mode of operation	load of Video amp	beam load	picture
case 1	load increases	load increases	bright
case 2	load decreases	load decreases	dark
case 3	load increases	load decreases	dark
case 4	load decreases	load increases	bright

Fig. 2.3

2.3 Video amplifier for compensation of beam current variations

Most of the commercial TV-sets show the effect that the beam power (e.g. 0 to 6 W) varies in the same direction as the video-amplifier does when different loads are applied, i.e. for a bright picture the total power dissipation is 10 W and for a dark one it is about 2 W (see **fig. 2.3**).

To reduce this disadvantage the following video amplifier concept is recommended for modern, fully transistorized TV-receivers. It is advantageous especially in the case where the load has to be taken over.

The video amplifier shown in **fig. 2.3.1** decreases the variable load from 10W to about 1 to 3W. Therefore picture seize variations as a result of different brightness changes will not occur with the same effect than before. In order to avoid load changes by the brightness, which is manually adjusted, the brightness potentiometer (2 kΩ) is connected infront of the picture output-amplifier transistor BF 457. If this potentiometer is adjusted the base and collector dc-voltages are shifted in relation to the basic brightness-adjustment (100 kΩ). The diode BA 127 keeps the voltage of the bridge (330/500/330 Ω) constant via the first transistor of the contrast adjustment circuit. Thus the contrast adjustment conditions do not inadmissibly vary, i.e. no picture brightness changes will happen. The sound-IF is picked up just behind the video diode AA 116 by a 5.5-MHz-bandpass filter. Thus the influence of the blanking pulses on the sound is kept low. The blanking of the horizontal fly-back is accomplished at the cathode of the picture tube and the one of the vertical fly-back is achieved at the emitter of the transistor BF 457. The 22-kΩ-resistor (drawn with dashed lines) improves the conditions at supply voltage fluctuations (120 V), because the stability of the adjusted average voltage between grid a cathode of the picture tube is increased.

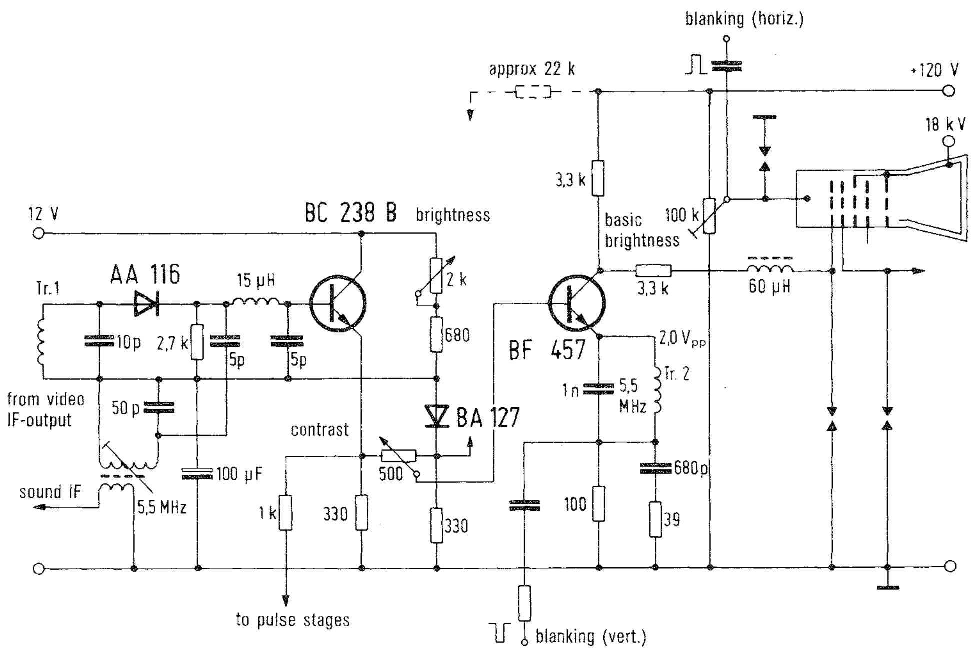


Fig. 2.3.1

The sparking gaps at the electrodes of the picture tube, the choke as well as the series resistor connected to the collector of the transistor BF 457 protect latter from picture-tube spark-overs.

It should be mentioned that npn-video-transistors require the described grid control, whereas for pnp-types the conventional cathode control of the picture tube can be used.

The latter method is more common, since most of the usual video amplifiers are equipped with npn and pnp transistors, whereby the given load conditions apply to case 1 as well as to case 2. If the video signal control phase is shifted by 180°, it is possible to realize the load conditions of case 3 and 4 when a video output stage with pnp-transistors is used. This is also achievable at a grid control of the picture tube, whereat a npn-transistor can be used furthermore.

The windings for the supply of the video signal should be placed under the high-tension winding (16 KV) of the horizontal transformer. Thereby the internal resistance of the high-tension source is decreased.

2.4 Parallel control devices for TV-sets

(see chapter 6.1)

2.5 Pulse-current-stabilized horiz.-deflection circuit with mains separation

TV receivers totally equipped with semiconductors are already available. Lately requests have been increasing to replace the heavy mains transformer, requiring an expensive chassis construction, by simpler and lighter equipment.

The pulse-deflection circuit with synchronized switch-mode power supply, shown in **fig. 2.5**, is a very simple solution, whereby the switch-mode power supply requires no separate transformer. The available high-tension transformer is used for it, as well as for the line voltage separation.

The "back-stroke-fed" horizontal-deflection circuit described below offers the following essential features:

1. minimum quantity of components,
2. supply voltage separation in the horiz.-transformer,
3. control of supply voltage fluctuations (190 to 250 V),
4. automatic generation of 30 V for other circuits of the TV-set,
5. secondary short-circuit protection through electronic switch-off,
6. protection of high-tension spark-overs in the picture tube,
7. no r.f.-interferences in the picture on account of back-stroke-feeding,
8. constant picture seize, independent of supply voltage fluctuations,
9. picture seize stabilization with regards to beam load changes is easily realizable,
10. simple 30-V-auxiliary voltage supply during repair,
11. mains or battery operation with booster is possible,
12. relatively low collector voltage required for the deflection transistor and the pulse transistor (< 400 V).

The new pulse-deflection circuit is almost ideal for the separation of primary and secondary influences on the picture-seize constancy, so that it is easy to take separate, effective, measures against these influences. Pulse-current stabilization is achieved by a particularly simple circuit controlling the power supply transistor BU 111.

On principle only the feedback voltage is clipped by a z-diode and fed to the base of the BU 111. At base and emitter a RC-circuit each obtains the control, which becomes effective only in the upper part of the pulse and thus greatly reduces switching losses (from 30 to 180 Watt). The resistor R_5 connected to the emitter limits the current and increases particularly the already high internal collector impedance.

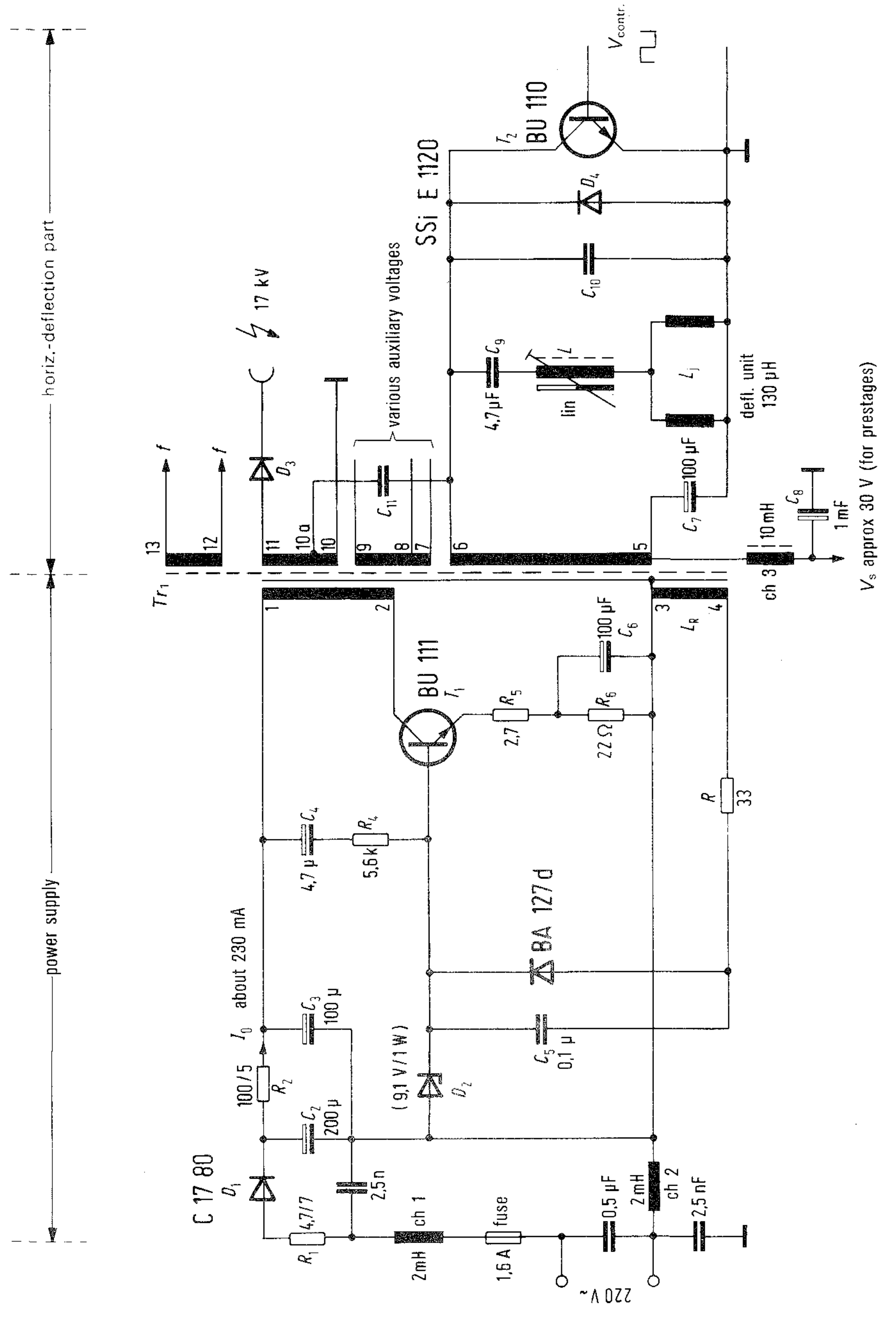

horiz.-deflection part
power supply
Tr_1
BU 111
BU 110
SSi E 1120
BA 127 d
C 17 80
various auxiliary voltages
17 kV
defl. unit
130 µH
V_s approx 30 V (for prestages)
I_0 about 230 mA
220 V~
fuse
1,6 A
ch 1
ch 2
ch 3
10 mH
1 mF
(9,1 V/1 W)
22 Ω
5,6 k
4,7 µF
100 µF
$V_{contr.}$

Fig. 2.5

The control action can be derived from the horizontal deviation of the load-dependent power triangle in the field of output characteristics. Thus supply-voltage fluctuations remain ineffectually as long as the transistor does not operate too far in the range of collector saturation.

This kind of load is permissible without any restrictions, because modern, triple-diffused transistors are able to stand relatively high power dissipations (50 W) in comparison to typical high-tension types (1500 V) which, for instance, are capable to carry only 12 Watt.

The power-loss behaviour of the edges and residual voltages is remarkable (figs. **2.5.1a, b, c**). The edge-power-losses, however, can be kept small by switching on the collector current only when the collector voltage has dropped to a sufficiently low value and when the current is turned off already, before the voltage rises again.

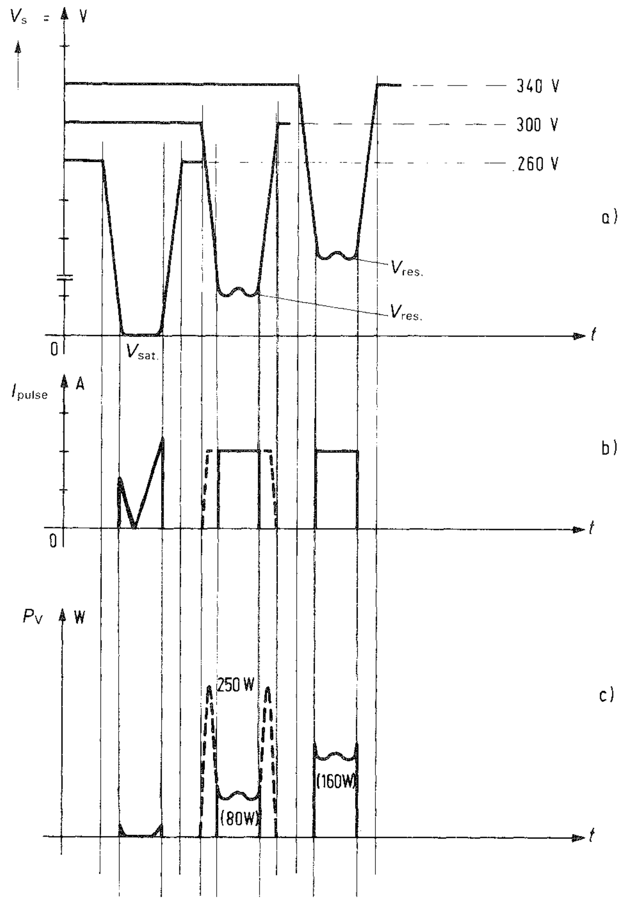


Fig. 2,5,1

This can be achieved by the following measures:

a) operating the emitter with a dc bias, i.e. control by the pulse peak (RC-circuit with great time constant connected to the emitter),

b) by a small value of the ratio: feedback-pulse voltage to z-diode voltage ($V_{R\,imp}$: $V_z \approx 1.4$),

c) by differentiation of the fly-back pulse, flowing towards the z-diode D_2, through a RC-circuit (R/C_5) or through a RL-circuit.

d) generation of appropriate edge counter-voltages by means of a suitable combination of components consisting of L, R, C and D in the collector circuit of the pulse transistor.

In these cases the transistor becomes conductive a few microseconds after the beginning of the fly-back. It is turned off a few microseconds before the fly-back is finished. The collector voltage has high levels especially at the beginning and the end of the fly-back, as it evident from **fig. 2.5.1**. Therefore it is advantageous to turn on the transistor only when the fly-back has passed its half distance. The cooling of the power supply transistor BU 111 should exceed the required minimum.

Through the starting-C_4-R_4-circuit a short current surge is supplied to the base of T_1 and at a voltage higher than 100 V the transistor begins to oscillate with a frequency of about 40 kHz. At about $V_{S\,sec}$ = 10 V for the prestages, the horiz.-generator operates so intensely that the frequency of the self-oscillating power supply transistor T_1 is pulled to the line frequency. The surge-starting combination effects an electronic protection of the circuit during secondary short-circuits.

2.6 Horizontal-generator with breakdown-proof driver

The horiz.-generator shown in **fig. 2.6** is a typical, conventional multivibrator, which allows to tune the frequency (15625 Hz) high-resistively. The influence, however, is achieved only from one side, because this guarantees that the transistor T_2 must not have a too high current gain (B>150).

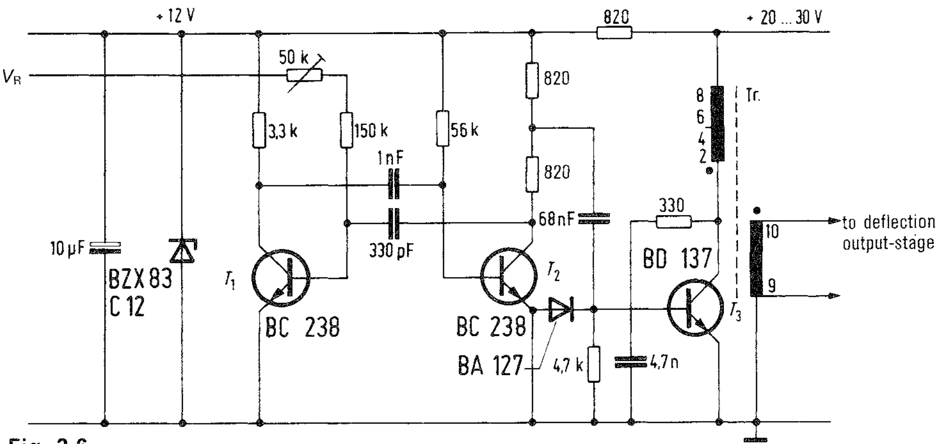


Fig. 2.6

The driver transistor T_3 is coupled through the 68-nF-capacitor. The negative amplitude of the oscillation is clamped to minus level to achieve that the capacitor can be discharged and thus sufficiently positive current can be supplied.

The driver transformer operates as a storage, i.e. the energy is converted during the transistor reverse period. Operation during the conductive period is also possible with the same results, but only the value of the protection resistor has to be decreased from 330 Ω to about 100 Ω.

The frequency constance of the described circuit is extremely good and is also improved by the 12-V-regulation of the z-diode. The value of the filtering capacitor (in this case 10 μF) determines the multivibrator's build-up time, which is less than 10 ms.

The table below shows how the horiz.-generator reacts during the beginning of oscillations. Besides that the necessary supply voltage is indicated for the base current required respectively (e.g. for portables, monochrome home TV-sets or colour-TV-receivers).

If the horizontal oscillation is disturbed the driver transistor is without current, i.e. neither the transistor T_3 nor the driver transformator can be damaged when the supply voltage V_S remains available.

Technical data

V_S	$1/f$	$I_{B(ZE)}$ for $R_B = 1\ \Omega$	$I_{B(ZE)}$ for $R_B = 0.68\ \Omega$	V_{CEV}
5	63	–	–	24
10	72	0.2	0.3	40
10	67	0.6	0.8	54
20	66	0.9	1.1	66
25	65	1.25	1.7	80
30	65	1.7	2.2	95

2.7 Vertical-deflection circuit with diac generator

The vertical-deflection circuit described in the following **(fig. 2.7)** permits the selective use as well for b/w portable TV sets as for home colour TV receivers without any essential change of components.

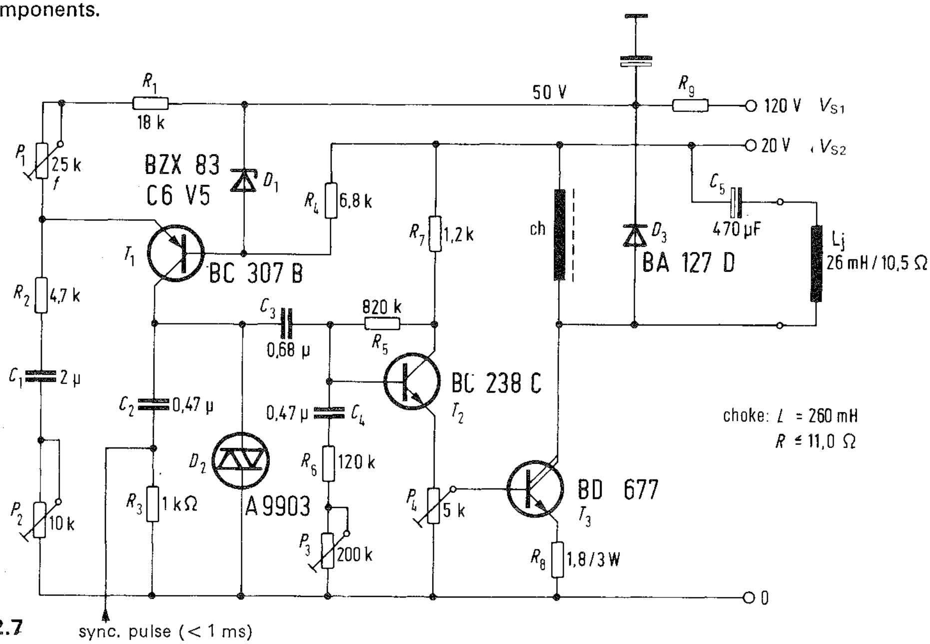


Fig. 2.7

Compared to common deflection circuits this one is simple and well-arranged. A trigger diode (diac) is used for the 50-Hz-sweep-generator which is forced to continue its oscillation even if there is a lack of picture pulses. The diac is triggered, e.g., at a voltage of 35 V and it is switched off at a voltage of about 20 V. In this case the alternating amplitude is about 10–15 V_{pp}.

The capacitor C_2 is charged through the constant current source consisting of the components T_1, D_1, P_1, R_1 and R_4, whereby the voltage across C_2 arises with constant slope as long as the firing voltage of the diac has been reached. D_2 becomes low-ohmic and discharges C_2 via R_3 rapidly (about 0.8 ms). A saw-tooth voltage is generated at the collector of T_1. It controls via C_3 the transistor T_2, which acts as an impedance transformer. The control current of the darlington transistor T_3 is adjusted by the potentiometer P_4. The collector current is supplied via the choke ch. The current flowing through the vertical-deflection coils is symmetrically to the zero axis and has the amount of 1 A_{pp}.

To correct the curve shape of the current function (slight S-shape) the total linearity can be adjusted through P_3. The initial linearity is set by the potentiometer P_2.

To be able to compensate tolerances of the diac, type A 9903, the frequency is adjustable within the ratio of 1:3 by the potentiometer P_1.

The diode D_3 limits the inductive voltage peaks to a value of e.g., 50 V to protect the transistor T_2. The resistor R_9 (about 16 to 22 kΩ, 0.3 W) reduces the video voltage to a value of 55 to 65 V, required by the generator. At the output capacitor C_5 a fully symmetrical parabola-voltage is available. In order to achieve a stable synchronisation of the diac-circuit pulses of about 2 to 5 V have to be supplied to the turn-off resistor of 1 kΩ.

Technical data

V_{S1}	Video supply voltage, about 120 V
V_{S2}	supply voltage for the vert.-deflection circuit, 20 V
I_S	supply current <0.6 A
P_{in}	power consumption <12 W
T_1	BC 307 B
T_2	BC 237
T_3	BD 677
D_1	BZX 83 C6 V5
D_2	A 9903
D_3	BA 127
Ch	current-feed choke EI 54–18 (n = 750 CuL 0.4, L = 260 mHy, 11 Ω) B71702-S57-A1
Lj	vert.-deflection-unit 26 mH/10.5 Ω

3. Circuits for colour TV-receivers

3.1 Vertical-deflection circuit for 110°-standard-neck tubes with delta configuration and for RIS-inline tubes

All components of the vertical-deflection circuit **(fig. 3.1)** are mounted on a pc board, devised as a plug-in unit, with the dimensions of 100×93 mm. The cooling plate for the transistors of the output stage covers totally the board and acts also as screening.

The total deflection circuit consists of the oscillator, the d.c.-coupled driver amplifier and the push-pull output stage. An additional transistor T_8 generates a negative pulse for the blanking during the fly-back.

The vertical-deflection module is favoured for 110°-standard-neck picture tubes with delta configuration and for RIS-tubes, seize 18″ to 20″. The values for the components and the voltages are put in parenthesis. The figures in the drawing indicate the pin number of the module.

The oscillator (T_1 and T_2) is synchronized through an integrating circuit with two sections R_1/C_1 and R_2/C_2. Its supply voltage is regulated by the z-diode D_2. The capacitor C_3 is discharged by a rectangular-shaped signal, which is available at the collector of the transistor T_2. During the charging the diode D_1 separates the charging capacitor C_3 from the actual oscillator. The charging of this capacitor is attained by a relatively high voltage from the horizontal-deflection circuit (about 800 to 1000 V). This voltage is current-dependent. This method offers two advantages:

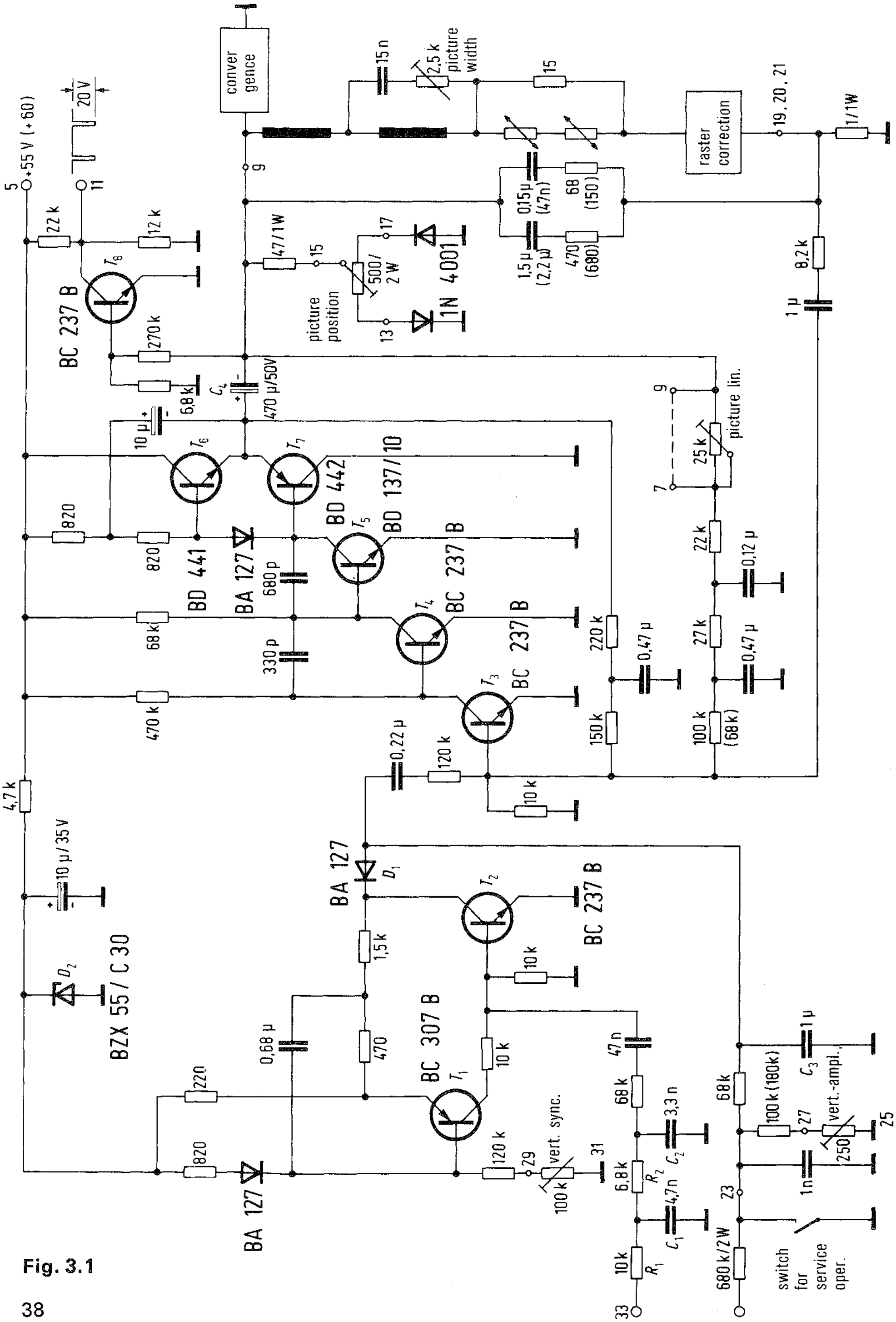
1. The charging can be achieved through a high series resistance, whereby the current remains practically constant. The saw-tooth voltage has a very constant slope.
2. If the beam current is enlarged the voltage available for charging the capacitor is diminished, i.e. the amplitude of the generated saw-tooth voltage is reduced. As it is well known the sensitivity of deflection is increased with decrease of the high-voltage, i.e. the picture amplitude would increase, if this effect is not compensated by the charging voltage which follows the change.

The saw-tooth voltage is amplified through a directly coupled four-stage amplifier and supplied to the deflection coils via the coupling capacitor C_4. The class B push-pull output stage of the amplifier operates with the complementary transistors BD 441 and BD 442. Due to the negative feedback, being very strong, no adjustment of the closed-circuit current is necessary.

The circuit generates a negative going saw-tooth voltage. The positive blanking pulse extends up to the supply voltage level of V_S = 55 (60) V. Unlike other vert.-deflection circuits, in which the blanking pulse is generated across the deflection coils, this circuit offers the advantage that the blanking pulse does not collapse (e.g. by a passive convergence circuit). Thus the fly-back time remains constant.

Technical data:

Supply voltage:	V_S	= 55 (60) V
Deflection current:	$I_{defl.}$	= 1.1 A_{pp} (1.3) A_{pp}
Power consumption:	P_{tot}	= 13 (18) W
Fly-back time:	t_r	= 0.9 ms
Deflection unit:	L_{tot}	= 25.4 mH
	R_{tot}	= 23 (8.2) Ω



conver gence
15 n
2,5 k picture width
15
raster correction
19, 20, 21
1/1W
5
+55 V (+60)
11
20 V
9
22 k
12 k
T8
BC 237 B
270 k
6,8 k
47/1W
15
picture position
500/ 2 W
17
13
1N 4001
0,15 µ (47n)
1,5 µ (2,2 µ)
68 (150)
470 (680)
8,2 k
1 µ
C4
470 µ/50V
10 µ
T6
T7
BD 442
BD 137/10
T5
BD 441
820
820
BA 127
680 p
BD 237 B
picture lin.
9
7
25 k
22 k
0,12 µ
68 k
T4
BC 237 B
330 p
220 k
0,47 µ
27 k
0,47 µ
470 k
T3
BC 237 B
150 k
100 k (68 k)
4,7 k
0,22 µ
120 k
10 k
10 µ/35V
BA 127
D1
T2
BC 237 B
D2
BZX 55/C 30
1,5 k
10 k
0,68 µ
470
BC 307 B
T1
10 k
220
47 n
68 k
1 µ
C3
vert.-ampl.
820
BA 127
120 k
29
vert. sync.
100 k
31
68 k
3,3 n
C2
6,8 k
R2
4,7 n
C1
10 k
R1
33
100 k (180 k)
27
250
25
1n
23
680 k/2W
switch for service oper.

Fig. 3.1

3.2 Horizontal-deflection circuit using BU 208 for 110°-standard-neck picture tubes with delta configuration and for RIS-inline-tubes.

A fundamental circuit for the horizontal deflection was already described in Design Examples of semiconductor circuits, edition 1974. The circuit shown in **fig. 3.2** uses additionally a pincushion-correction circuit and a picture-width plug. With the new line transformer AZ 3102 a lower internal impedance of the high-tension source is achieved by tuning of the high-tension coil.

By means of the picture-width plug the picture width can be varied, whereby the high-tension remains nearly constant.

The circuit using the line transformer AZ 3102 is favoured as well for 110°-standard-neck picture tubes with delta configuration as for RIS-inline picture tubes. Only the fly-back capacitance has to be reduced, the series resistance of the power supply line has to be increased somewhat and a different pincushion correction circuit has to be used. The values for the RIS-tube are indicated in parenthesis.

The BU 208 is operated as a common-base circuit as shown in **fig. 3.2**. Its emitter is controlled via the transistor T_2. Thus an accurate switching is attained.

The positive driving pulse of the TBA 920 turns on the transistor T_3 being non-conductive up to that time. The transistor T_2 was switched off, because of its connection to the auxiliary supply voltage of +5 V via the 15-Ω-resistor. The transistor T_2 is now turned off. The emitter current of the BU 208 charges the 0.68-μF capacitor up to its maximum value. The reverse base control current of the BU 208 flows to ground via the resistor of 2.7 Ω, the capacitor of 25 μF and the resistor of 1 Ω. This takes about 3 μs and after that the BU 208 switch off with a decay time of about 0.7 μs. The 0.68-μF-capacitor connected from emitter to ground is essential in order to guarantee a clean switching.

When the set is switched on, the base current of the BU 208 flows from the +17-V-supply via the resistor of 220 Ω. Under operating conditions, however, it flows from the auxiliary supply of +5 V via the resistor of 2.7 Ω. As emitter-load transistor the epibase type BD 435 in plastic case is particularly suited because of the extremely low saturation voltage of 1 V at 4 A.

Protection circuit

The protection circuit consisting of the transistors T_3 and T_4 prevents a damage of the line output-stage transistors when short-circuits or picture-tube flash-overs occur.

The voltage drop across the emitter resistor of 1 Ω is proportional to the collector current of the BU 208. If this voltage exceeds the "protection level", adjusted through the 100-Ω-resistor, then the transistor T_4 becomes non-conductive. The transistor T_5 becomes conductive and turns on the driver transistor T_3, the transistors T_1 and T_2 are switched off. The resetting happens automatically after a time of several milliseconds, i.e. when the 0.68-μF-capacitor is discharged via the 3.9-kΩ-resistor. To protect the output-stage transistor safely also against short surge currents a RC-circuit with two time constants (2.2 nF/47 Ω – 6.8 μF) is connected to the base of transistor T_4.

Pincushion correction circuit

For the north-south and the east-west corrections only a 30-mm-transductor, type AZ 3410 M (AZV 340), is used. Both correction circuits can be adjusted independently. An harmonic filter circuit, consisting of AZ 3525 and two capacitors (330 nF/47 nF), is added to compensate the s-shaped distortions, the so-called "moustache" distortions. The phase is adjustable through the coil AZ 3525.

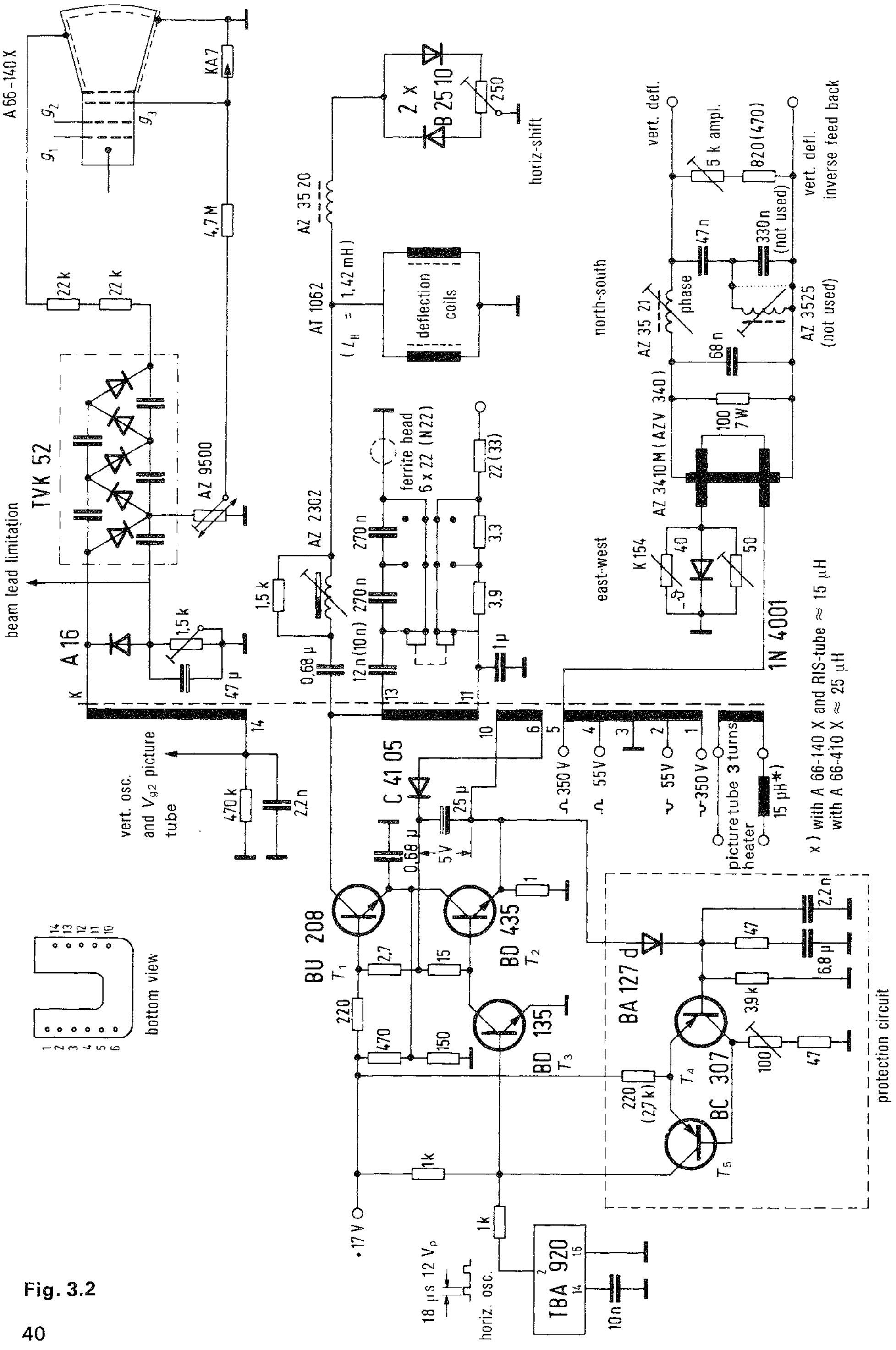

A 66-140 X
KA7
4,7 M
22 k
22 k
TVK 52
AZ 9500
beam lead limitation
A 16
1,5 k
47 μ
K
14
vert. osc. and V_{g2} picture tube
470 k
2,2 n
2 x B 25 10
250
horiz-shift
AZ 35 20
AT 1062
L_H = 1,42 mH
deflection coils
ferrite bead 6 x 22 (N22)
22 (33)
3,3
3,9
1 μ
AZ 2302
270 n
270 n
12 n (10 n)
0,68 μ
1,5 k
13
11
10
6
5
north-south
east-west
vert. defl.
5 k ampl.
820 (470)
vert. defl. inverse feed back
47 n
330 n (not used)
phase
AZ 35 21
AZ 3525 (not used)
68 n
100 7 W
AZ 3410 M (AZV 340)
K 154
40
50
1N 4001
350 V
55 V
55 V
350 V
picture tube 3 turns
15 μH*)
picture tube heater
x) with A 66-140 X and RIS-tube ≈ 15 μH
with A 66-410 X ≈ 25 μH
C 41 05
25 μ
0,68 μ
5 V
BU 208
T_1
BD 435
T_2
BD 135
T_3
BA 127 d
BC 307
T_4
T_5
2,7
15
220
470
150
1
2,2 n
47
6,8 μ
3,9 k
100
47
220 (2,7 k)
1k
1k
protection circuit
+17 V
TBA 920
10 n
18 μs 12 V_p
horiz. osc.
bottom view

Fig. 3.2

The combination-transductor is premagnetized through the diode 1 N 4001. The east-west correction can be adjusted by the 50-Ω-resistor connected in parallel to the diode and the NTC-resistor, type K 154, which is responsible for the temperature compensation. If it is required, the quality of the "inner-pincushion"-correction can be improved by the rotatable, permanent-magnet. Although the correction circuit does not inductively load the fly-back transformer, neither a disadvantageous high-tension modulation occurs nor a pincushion-correction dependency on the beam current is evident. This fact is especially achieved by the compensating effect of the 22(33)-Ω-resistor inserted in the power supply line. The adjustment of the pincushion correction is to be made in the following sequence:

1. all adjustors to mid-position, turn out the core of the AZ 3525 as far as possible,
2. adjust the east-west correction through the 50-Ω-potentiometer and correct it by the permanent-magnet,
3. adjust north-south phase, through AZ 3521,
4. adjust north-south amplitude by the 5-kΩ-potentiometer,
5. optimize the pincushion correction by means of the harmonic filter circuit (AZ 3525); this is not necessary with RIS-tubes.

The pincushion-correction circuit is mounted totally on a plug-in pc board with the dimensions of 50×85 mm. It is available under the ordering code AZB 3000 (AZB 3001).

Test results of a horiz.-deflection output stage with the deflection unit AT 1062 for standard-neck picture tubes.

Beam current	I_b	0	0.1	1.2	1.5	mA
Nominal supply voltage	V_s	150	150	150	150	V
DC voltage at terminal 11 of the horiz.-transformer		132.5	132	127	125	V
Supply current	I_{tot}	500	510	685	725	mA
High tension	$V_{h.t.}$	25.7	25	22.6	22	kV
Picture width	B	100	100.6	101.8	101.8	%
Fly-back voltage at the horiz.-defl. unit	V_y	1320	1320	1280	1280	V
Fly-back time	t_r	10.5	10.5	10.6	10.6	µs
Deflection current	I_{defl}	6.0	6.0	5.8	5.8	A_{pp}
Internal resistance 0.1 to 1.5 mA	R_i	–	–	2.1	–	MΩ
BU 208						
Collector peak current	$+\hat{I}_c$	4.4	4.4	4.2	4.2	A
Inverse collector peak current	$-\hat{I}_c$	3.3	3.3	3.1	3.0	A
Collector peak voltage	$\hat{V}_c$	1240	1240	1160	1150	V
Collector total power dissipation	P_c		3–8.5*)			W
Storage time	t_s	3.2	3.2	3.0	2.9	µs
Switch-off time	t_{off}		0.5–1.6*)			µs
BD 435						
Collector peak current	$+\hat{I}_c$	5.1	5.1	5.1	5.1	A
Collector inverse peak current	$-\hat{I}_c$	1.1	1.1	1.0	1.0	A
Collector peak voltage	V_{CE}	18.0	18.0	17.0	17.0	V

*) depends on B and switching time of BU 208

Test results of a h-deflection output stage driving a RIS-tube with a deflection unit of L_H = 1.42 mH

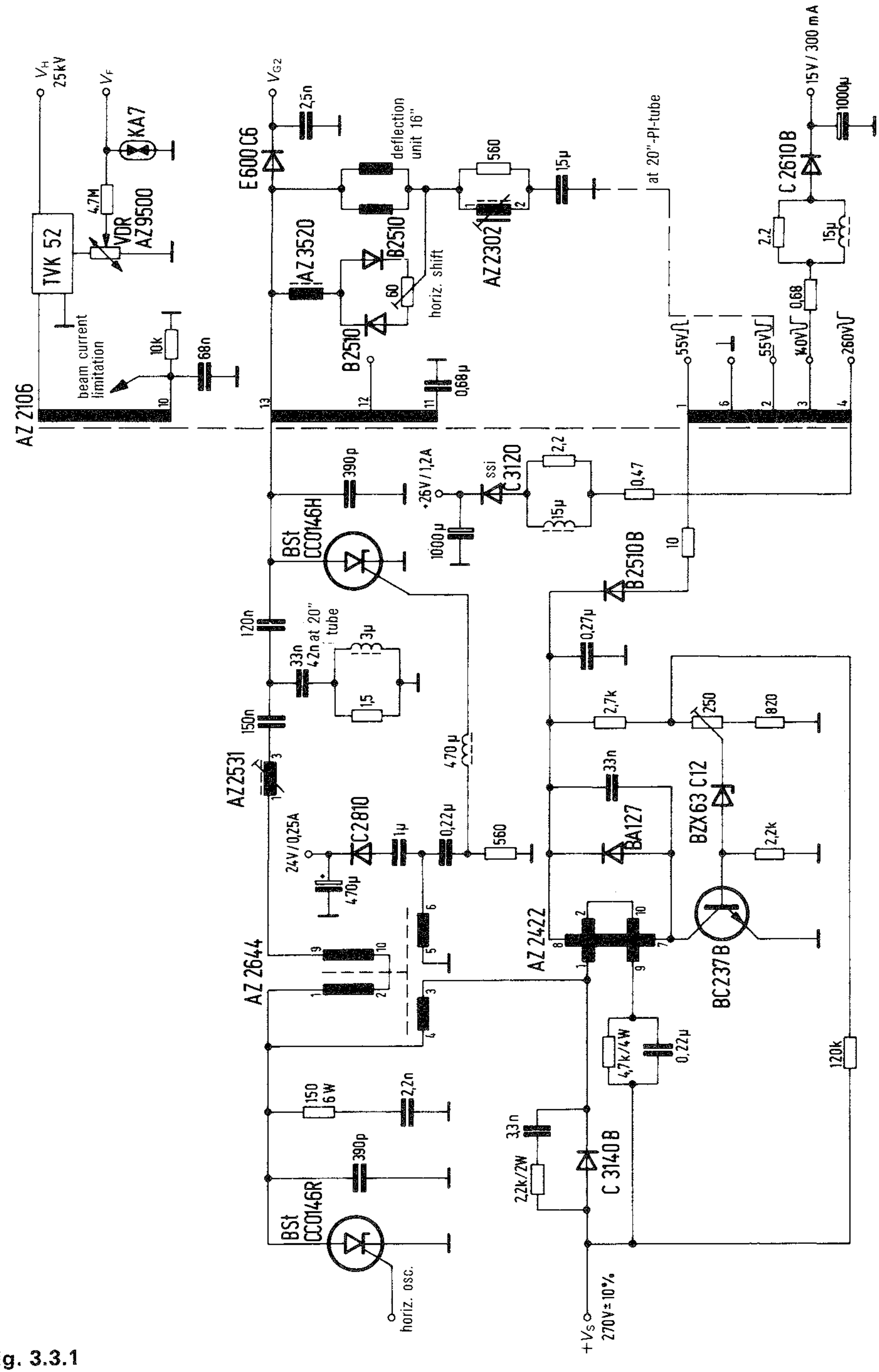
Beam current	I_b	0	0.1	1.2	mA
Supply voltage	V_S	150	150	150	V
DC voltage at terminal 11 of horiz. transformer		132	132	130	V
Supply current	I_{tot}	540	550	620	mA
High-tension	$V_{n.t.}$	25.7	25.3	23.7	kV
Picture width	B	100	100.6	101.5	%
Fly-back voltage at horiz.-defl.-unit	V_y	1360	1360	1320	V
Fly-back time	t_r	10.3	10.3	10.4	μs
Deflection current	I_{defl}	5.1	5.1	5.0	A_{pp}
Internal resistance 0.1 to 1.5 mA	R_i	–	–	1.44	MΩ
BU 208					
Collector peak current	$+I_c$	4.3	4.3	4.2	A
Inverse collector peak current	$-I_c$	3.2	3.2	3.0	A
Collector peak voltage	V_c	1200	1200	1180	V
Collector power dissipation	P_c		3–8.5*)		W
Storage time	t_s	3.8	3.8	3.7	μs
Switch-off time	t_{off}		0.5–1.6*)		μs
BD 435					
Collector peak current	$+I_c$	5.0	5.0	5.0	A
Inverse collector peak current	$-I_c$	1.0	1.0	0.9	A
Collector peak voltage	V_{CE}	18.0	18.0	17.0	V

*) depends on B and switching time

3.3 Line-sweep circuits and high-tension generation using thyristors

The circuits for standard-neck and thin-neck colour picture tubes described already in Design Examples of Semiconductors Circuits, edition 1974, section 3.7, are now modified to meet the requirements of the modern in-line picture tubes (PI/90°, 16″ and 20″ as well as RIS/110°, 18″ to 22″).

As the thyristor output stages **(fig. 3.3.1** and **3.3.2)** are stabilized against load and mains variations by way of the well known control transductor AZ 2422, they can be operated by a very simple devised power supply using a half-wave rectifier. The other stages of the TV-set are provided from the line transformer. For rectification of the RF-pulses fast silicon diodes are required (e.g. B 2510, C 2610 B, C 2810).



TVK 52
VDR
AZ 9500
KA7
E600 C6
AZ 3520
B2510
AZ 2302
deflection unit 16"
horiz. shift
at 20"-PI-tube
beam current limitation
AZ 2106
C 2610 B
C 3120
BSt CC0146H
B 2510 B
AZ 2531
C 2810
AZ 2644
AZ 2422
BA 127
BZX 63 C12
BC 237 B
C 3140 B
BSt CC0146R
horiz. osc.
270 V ± 10%
15 V / 300 mA
+26 V / 1,2 A
24 V / 0,25 A

Fig. 3.3.1

The total pincushion correction is achieved by only one transductor passively controlled (not shown in the figures).

The line transformers AZ 2106 (**fig. 3.3.1**) and AZV 217 (**fig. 3.3.2**) are dimentioned so that a constant picture width as well as a low impedance of the high-tension source is attained for all conditions of standard operation by use of the selenium cascade TVK 52.

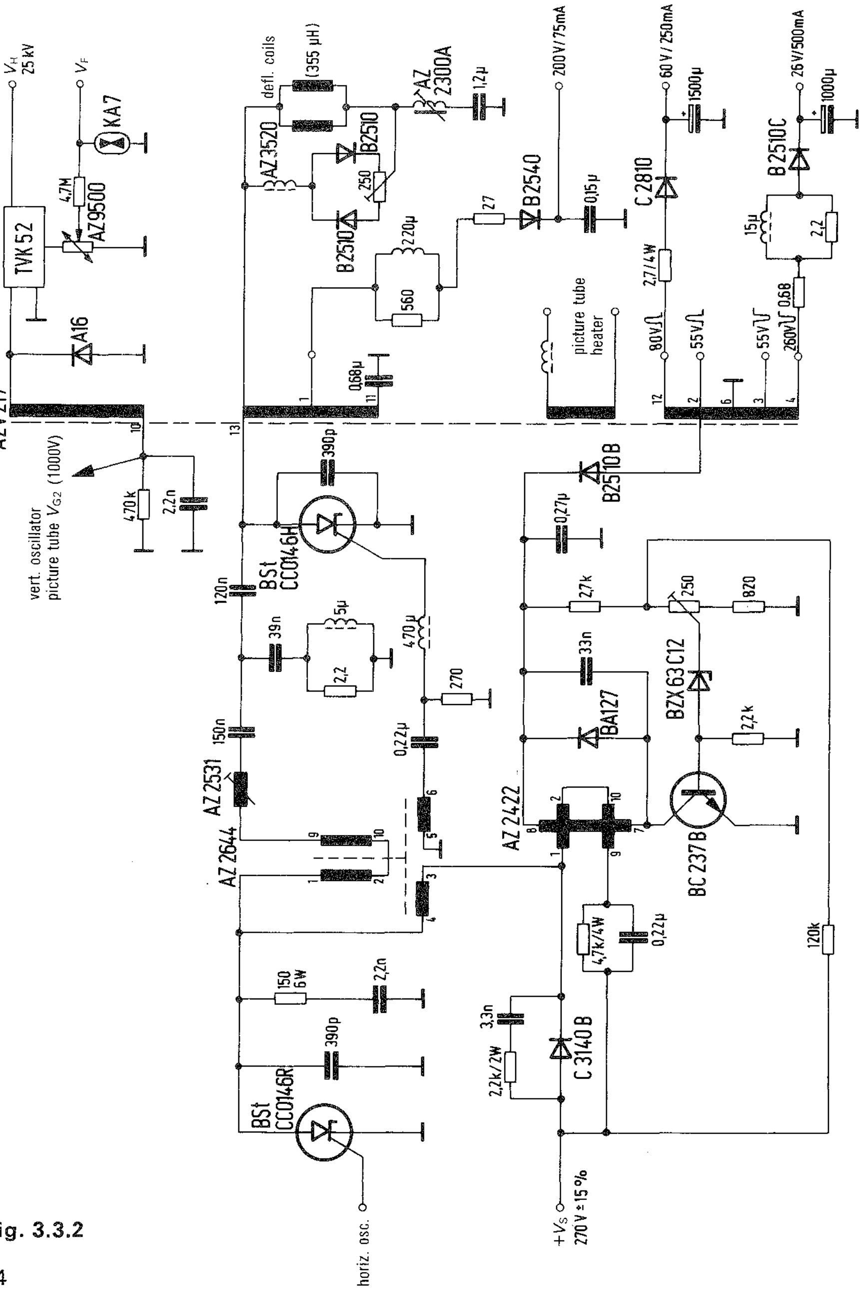


Fig. 3.3.2

Test results and data

	PI 16"/20" (fig. 3.3.1)	RIS 18"/22" (fig. 3.3.2)
Supply voltage	220 V ±15%	220 V ±15%
Operating voltage for the output stage with one-way rectifier C 1780	270 V non-regulated	270 V non-regulated
Inductances of the horiz.-coils	632 μH/664 μH	355 μH
Horiz.-defl. current	5.9 A_{pp}	10 A_{pp}
Horiz.-defl. voltage (fly-back)	680 V_{pp}/710 V_{PP}	630 V
Fly-back time	11.2 μs	11.2 μs
Internal resistance of the high-tension source	about 1.4 MΩ	about 1.6 MΩ
High-tension	25 kV	25 kV
Auxiliary pulses for other supplies	± 55 V_{pp}	± 55 V_{pp}
	±260 V_{pp}	±260 V_{pp}
	−140 V_{pp}	+ 80 V_{pp}

3.4 RGB-module

Because of the new picture-tube concepts at which the control grids do not have separate terminals, the tendency towards RGB-control of the picture tube is clear.

A RGB-control circuit **(fig. 3.4)** with black-level clamping in the output stage offers the advantage that the output circuits of the colour-decoder do not require any special actions for temperature-effect compensation. With circuits for blanked-signal-operation, the requirements for a hum-free power supply voltage are essentially lower.

The circuit described in the following is mounted on a plug-in pc board with the dimensions of 100×85 mm.

The inputs of the RGB-module are proportioned in the way that they will meet the colour difference output signal of the TAA 630 S and the luminance output signal of the TBA 560. The colour difference signals are available at the bases of the amplifier transistors BC 237 and the luminance signal, coupled via the common-emitter circuit with BC 307, is available at the emitters of the transistors BC 237. The primary signals are obtained by substraction:

$$(R-Y)+Y = R$$
$$(G-Y)+Y = G$$
$$(B-Y)+Y = B$$

These amplified, primary signals are available at the BC 237-collector resistors, consisting of a 2.5-kΩ-potentiometer and a fixed resistor of 470 Ω. A capacitor of 10 pF is connected between base and ground to reduce the influence of the "Miller"-capacitance between base and collector and to improve the frequency response which is not effected essentially by this capacitance. The primary signals are coupled to the output stages via electrolytic capacitors of 2.2 μF.

Three common-emitter circuits with BC 237 are connected infront of the output-stage transistors to achieve a sufficiently high input-impedance for the clamping circuit and to compensate the current-gain tolerances of the BF 458. The current gain of the output stages is determined by the ratio of the collector resistance and the emitter resistance. The latter is connected in parallel to a 1-nF-capacitor, which corrects the frequency response. Other equalizing components (peaking coil of 55 μH connected in parallel to a 3.9-Ω-resistor) are inserted in the cathode feed-line of the picture tube.

The operating point of the output stage is adjusted by the 330-kΩ-resistors, causing a positive base-current of the output-stage darlington-transistors.

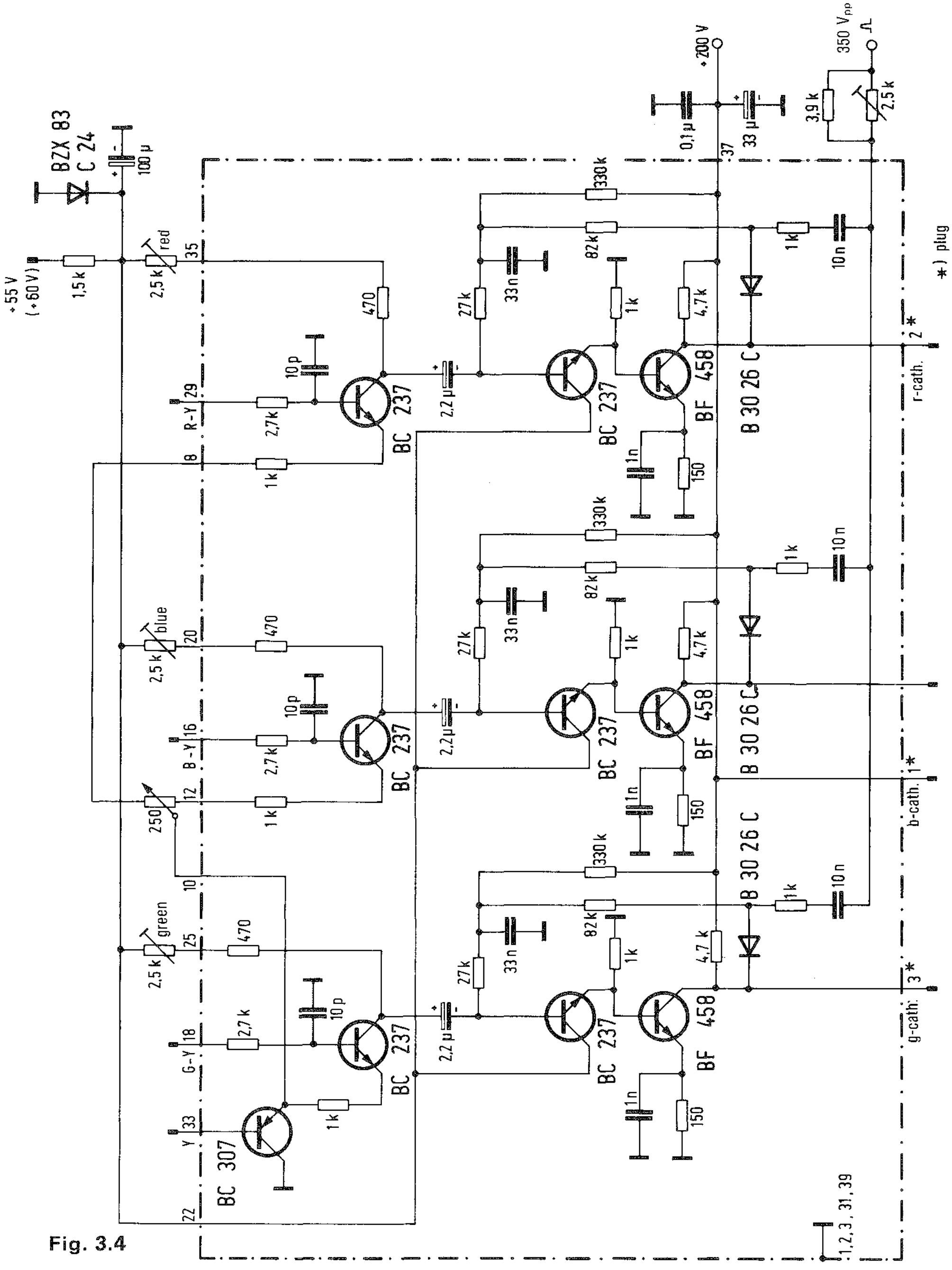

BZX 83
C 24
100 µ
+55 V
(+60 V)
1,5 k
2,5 k
red
blue
green
250
470
10 p
2,7 k
1 k
R-Y
B-Y
G-Y
Y
BC 237
BC 307
2,2 µ
27 k
33 n
82 k
330 k
4,7 k
150
1 n
10 n
BF 458
B 30 26 C
+200 V
0,1 µ
33 µ
3,9 k
350 V_pp
r-cath.
b-cath.
g-cath.
*) plug
1,2,3, 31,39

Fig. 3.4

An unsymmetrical circuit, using a dc clamp diode, is provided for the black level clamping. During the fly-back, having always a defined video-signal level, the clamp pulse charges the 10-nF-capacitor. If the pulse has decayed, a voltage with 0-level is practically available at one plate of the capacitor. On the other (upper) one there is a negative voltage, supplied as a controlled variable to the base of the output-stage darlington-transistors via a 82-kΩ-resistor and a filter section. This inverse current, which depends on the deviation from the actual black level, eliminates a part of the positive current flowing through the 330-kΩ-resistor.

The black level can be adjusted by the 2.5-kΩ-potentiometer which varies the amplitude of the blanking pulse.

It is convinient to connect a protective resistor of about 3.9 kΩ in parallel to the potentiometer to guarantee the existence of blanking pulses, even if the potentiometer should fail. Thus a self-heating of the output stages is avoided.

Required levels

Luminance signal	V_y	=	2 V_{pp}
Colour difference signal	$-V_{(R-y)}$	=	4 V_{pp}
Colour difference signal	$-V_{(G-y)}$	=	2.4 V_{pp}
Colour difference signal	$-V_{(B-y)}$	=	5 V_{pp}
Output signal	$V_{R,G,B}$	=	100 V_{pp}

Supply voltage

for prestage	V_s	=	24 V, 30 mA
for output stage	V_s	=	200 V

3.5 Video-IF-module with TBA 440 N/P

The integrated circuit TBA 440 N/P comprises a high-gain regulated video amplifier, a controlled demodulator, two low-impedance video outputs with complete key control as well as a delayed tuner control. At both types the black and white levels are adjustable separately. The white levels of video signals at positive and negative video output are independent of supply voltage. An internal temperature stabilization guarantees a trouble-free operation at ambient temperatures between −25 and +60 °C.

Both types differ only in the polarity of the control voltage of the tuner prestage

TBA 440 N is suitable for npn-transistors

TBA 440 P is favourable for pnp-transistors.

At both types a sufficient current is available at pin 5. Therefore all PIN-diode attenuators common today can be controlled directly without using additional transistors.

Fig. 3.5 shows the circuit of the complete video-IF-module mounted on a plug-in pc board with the dimensions of 50 × 90 mm. The IF of the mixer is supplied to pin 18 of the pc board and coupled to the pre-amplifier transistor BF 199 by a 27-pF-capacitor. This transistor separates the tuner from the video-IF-compact-filter and compensates the pass-band attenuation of such a filter. The collector of the pre-amplifier transistor is connected to the coil L_{D1} through a 22-Ω-resistor. The trap circuits for the frequencies 31.9 MHz, 33.4 MHz and 40.4 MHz are arranged in a bridge configuration. To the coil L_{D8} an additional coupling winding is attached for controlling the TBA 440 N/P.

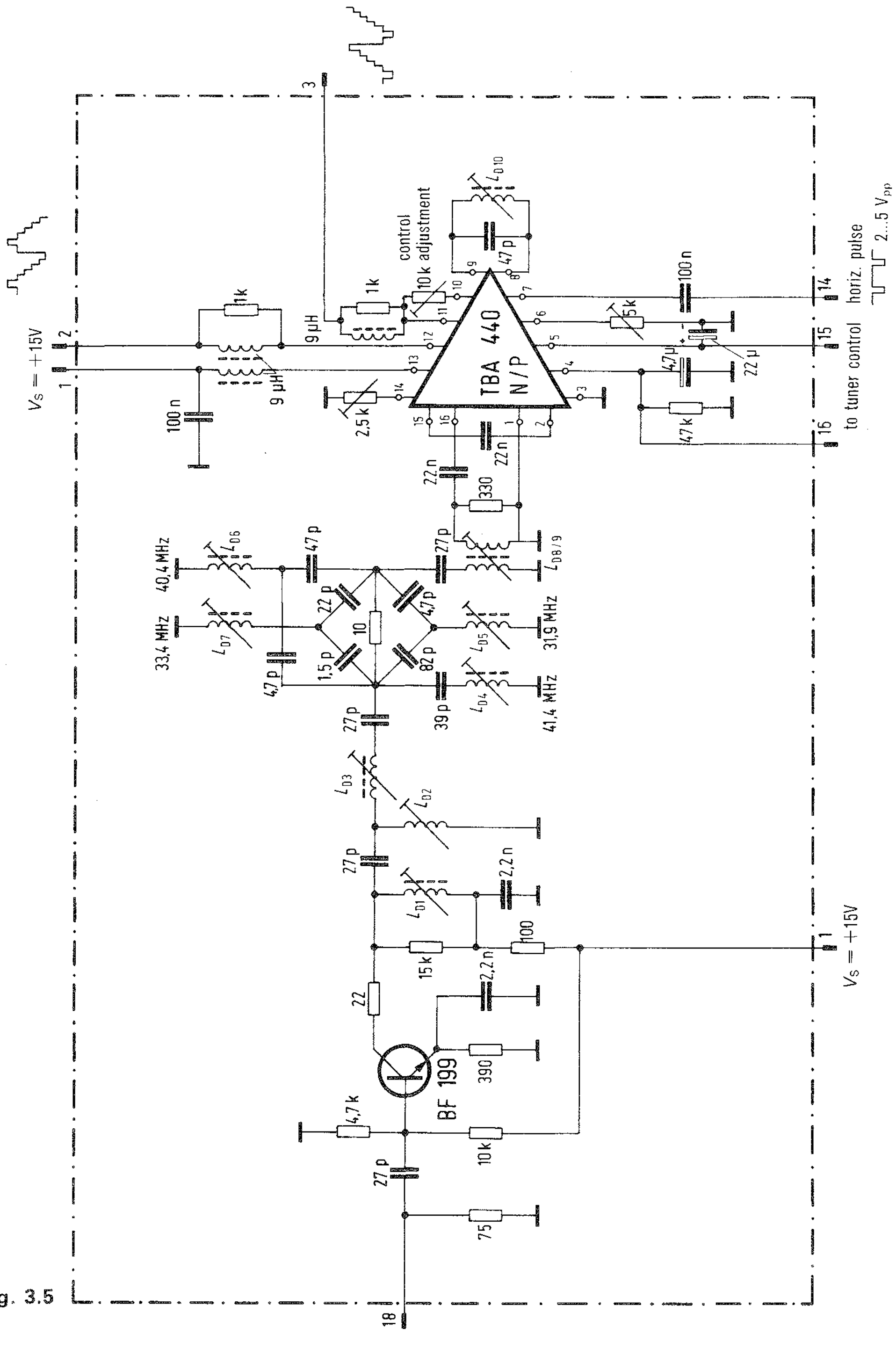

TBA 440 N/P
BF 199
$V_S = +15V$
control
10 k adjustment
horiz. pulse
2...5 V_{pp}
to tuner control
40,4 MHz
33,4 MHz
31,9 MHz
41,4 MHz
L_{D1}
L_{D2}
L_{D3}
L_{D4}
L_{D5}
L_{D6}
L_{D7}
$L_{D8/9}$
L_{D10}
9 µH

Fig. 3.5

The compact-filter is aligned in the conventional manner, whereby the demodulator resonant-circuit has to be damped through a 100-Ω-resistor. First the traps are adjusted. Then the edges and tilts are aligned by $L_{D\,1}$, $L_{D\,3}$ and $L_{D\,8/9}$. The left edge and thus the pass-band attenuation of the trap can be corrected by reducing the inductance of $L_{D\,2}$, i.e. by spreading apart the windings.

An auxiliary filter circuit, tuned to carrier frequency of 38.9 MHz, is connected to the output of the internal limiter amplifier, being part of the IC (pin 8 and 9).

In the leads of the video output and the power supply voltage filter chokes of 9 μH are inserted. The chokes of the video outputs are shunted by a 1-kΩ-resistor to improve the building-up behaviour.

The basic level without any video signal, i. e. without the white level, is adjusted through a 25-kΩ-potentiometer at pin 14 of the IC. The sync. level of the keyed control is adjustable through the 10-kΩ-potentiometer at pin 10. The tuner delayed control can be set by the 5-kΩ-potentiometer at pin 6. For the internal key-control, a negative line fly-back pulse of 2 to 5 V_{pp} has to be supplied to pin 7 via a capacitor of 100 nF. The RC-circuit (47 kΩ/4.7 pF) of pin 4 determines the time constant of the key-control. To achieve an operation of the video-IF-amplifier without any self-oscillation, the filtering capacitor of 22 nF, being responsible for the internal inverse feedback, has to be connected to the IC-terminals 2 and 15 as close as possible.

The supply voltage is 15 V. For max. 1 min a voltage of 16.5 V is admissible. The supply current at pin 11 and 15 should not exceed 5 mA flowing to ground or minus 1 mA to plus pole.

The coils $L_{D\,1}$ to $L_{D\,10}$ are available from the company Toko.

3.6 Colour processing

All components of the colour processing module, comprising a luminance and a controlled chrominance amplifier, a PAL-decoder, a reference oscillator and a synchronous demodulator, are mounted on a plug-in pc board with the dimensions of 100 × 100 mm. The integrated circuits TBA 560, TBA 540 and TAA 630 S are used. The transistor BC 338 reduces the supply voltage from 17 V to 12 V, required by the IC. The voltage is regulated by means of the z-diode BZX 83 C 12 **(fig. 3.6).**

The TBA 560 contains the luminance pre-amplifier. The control with the composite video signal at the input (pin 3) is an impressed-current-operation, because of the low input resistance. For a linear control the input current ranges between 0 and 2.5 mA. The matching to the y-delay line, connected infront, is achieved by the resistor R_1 = 1 kΩ. After the luminance signal has passed the internal input stage of the IC, it is supplied to a so-called "electronic potentiometer". The contrast can be set by a dc voltage at pin 2. The slider-terminal of the contrast potentiometer is connected to a RC-circuit (1.5 kΩ/47 μF) via the z-diode BZX 83 C 7 V 5. The RC-circuit generates a voltage which is proportional to the beam current. If this voltage exceeds the z-voltage of the diode, the dc voltage for the contrast control changes into negative direction. Due to the contrast-decrease, thus caused, this circuit operates as a beam-current limiter. The luminance amplifier offers at its output a clamped pedestal level. This is achieved by the following measure. When the luminance signal has passed the electronic potentiometer, the back porch is blanked by a gate-circuit, and this blanked value is stored in the capacitor C 1. This actual value is compared with a desired one, which is adjustable. A correcting variable is achieved in accordance to the difference. This variable is supplied to a controlled system

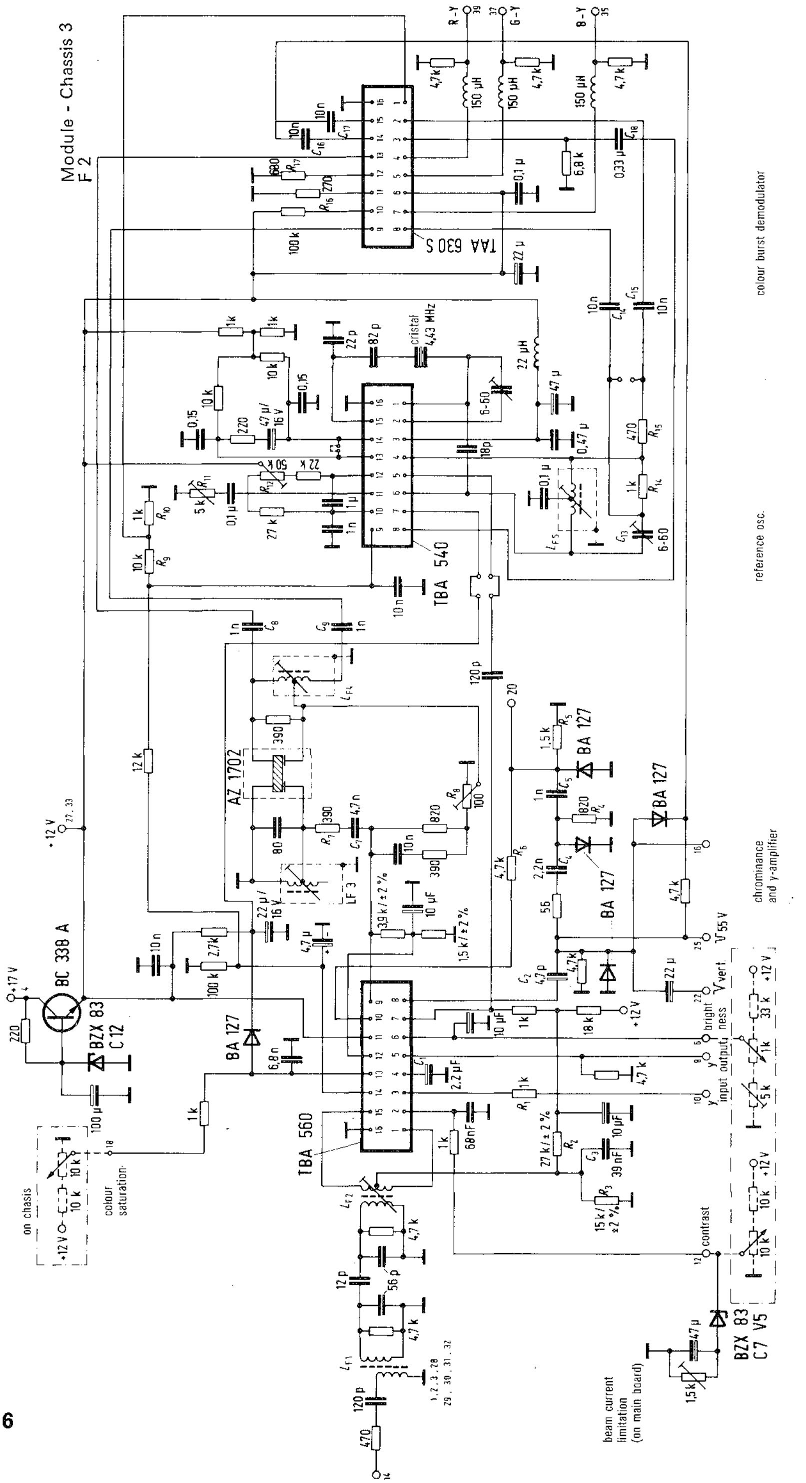

Module - Chassis 3
F 2
R-Y
G-Y
B-Y
TAA 630 S
TBA 540
TBA 560
cristal 4,43 MHz
AZ 1702
BC 338 A
BZX 83 C 12
BZX 83 C7 V5
colour burst demodulator
reference osc.
chrominance and y-amplifier
on chassis
colour saturation
brightness
y output
y input
contrast
beam current limitation (on main board)

Fig. 3.6

which reduces the difference between actual and desired value. As blanking pulse the burst gating pulse is used. For the contrast control a dc voltage is supplied to pin 6. It affects the controlled system of the black-level clamping. During the picture and line fly-back the luminance signal is blanked. This is achieved by supplying a negative, vertical blanking pulse to pin 22 and a negative, horizontal one to pin 25 of the module. Both pulses are added and are fed to pin 8 of the IC via the capacitor C_2.

The chrominance signal is supplied to the 4.43-MHz-filter (L_{F1}, L_{F2}) at terminal 14. It is symmetrically coupled to the IC by means of a coupling-winding, which is tapped to feed an inverse-feedback circuit for the internal dc voltage stabilization. The resistance ratio of R_1 and R_2 has to be kept very accurately. With reference to an ac voltage-operation the center-tap is connected to ground via a capacitor C_3. The crominance amplifier contains three electronic potentiometers in series. The first one achieves the chrominance control, the second one is responsible for the colour-saturation control and the third one is coupled with the contrast control of the luminance amplifier. The voltage for the contrast control affects the amplitude of the luminance signal and the chrominance signal in the same way. The tracking is better than 1 db over a control range of 10 db. The luminance signal and the chrominance signal are blanked during the picture and line fly-back.

The separation of the burst from the other part of the chrominance signal is obtained through two gates connected in series. The first one opens during the blanking of the chrominance signal, the second one is open only during a shorter time period of about 5 μs, i.e. during the back porch of the burst. Both pulses–for the blanking and for the burst gating–have to overlap. The burst gating pulse is derived from the trailing edge of the line pulse through a double-differentiating circuit, consisting of the two capacitors C_4, C_5, the two resistors R_4, R_5 and the two diodes BA 127. The resistor R_6 is required, since pin 10 of the IC is reserved for impressed-current-operation. The "burst", now being separated is picked up at terminal 7 and supplied to the TBA 540 via the capacitor C_6. It is used to synchronize the reference carrier. From its value a control voltage is derived and delivered to pin 14 of the TBA 560 via a filter circuit. This control voltage as well the burst signal as the chrominance signal, supplied at pin 9, is kept constant.

The controlled chrominance signal (pin 9) is supplied to the primary input of the ultrasonic delay line, type AZ 1702, via the capacitor C_7 and the resistor R_7. It is delayed by the time of one line, added and subtracted with the direct signal (delay-time-demodulator). Thus the both subcarrier-frequency signals F(B–Y) and F(R–Y) are achieved. They are supplied to the synchroneous demodulator via the capacitors C_8 and C_9. For the addition and for the substraction the direct signal as well as the delayed one must have the same amplitude. To compensate the residual attenuation of the glass delay-line a voltage divider is used. It can be accurately adjusted through the potentiometer R_8.

The chrominance-subcarrier reference signal is generated by a cristal oscillator. This signal and the "burst" are supplied to a phase comparison circuit, which creates the control voltage for the reactance circuit. This control voltage is filtered through the capacitors C_{10} and C_{11} as well as through the RC-circuit R_{13}/C_{12}. The reactance circuit tunes the subcarrier frequency, created by the cristal oscillator, to the exact frequency of the chrominance subcarrier, transmitted in addition to the burst from a TV-station. These functions are comprised within the IC TBA 540. Besides that this IC generates also the control voltage for the chrominance amplifier. Its value is derived from the burst, and it is adjustable through the potentiometer R_{11}.

The unfiltered control voltage contains also the PAL-identification signal which is supplied via the voltage divider R_9, R_{10} to pin 1 of the IC TAA 630 S in order to correct the PAL flip-flop. If there is no burst, alternating from line to line by ±45°, the IC TBA 540 generates a switching voltage (pin 7), which attenuates the colour saturation (colour killer). The threshold of the colour killer circuit is adjusted by potentiometer R_{12} (50 kΩ).

At pin 4 and 6 the frequency of the reference oscillator is available with a phase shift of 180° (refered to ground). The reference (R–Y) can be picked up at pin 4. It is supplied to pin 2 of the TAA 630 S via the resistor R_{15} and the capacitor C_{15}. The colour subcarrier reference signal (B–Y) has to be dephased by 90° refered to the reference signal (R–Y). This is achieved by the RC-circuit C_{13}, R_{14}. The signal is fed to pin 8 of the TAA 630 S via the capacitor C_{14}.

The TAA 630 S contains the synchroneous demodulator. The processed and controlled chrominance signal is supplied to pin 9 and 13, whereby the reference signals are fed to pin 2 and 8 as already mentioned above. The 180°-shift of the (R–Y) reference carrier signal is obtained by an internal PAL switch, which is controlled by supplying a line fly-back pulse to pins 14 and 15 via the capacitors C_{16} and C_{17}. The correct phase shift is set by the identification pulse at pin 1. From pin 3 a signal with half-line frequency is fed to pin 8 of the TBA 540 via the capacitor C_{18}. The correct operation of the PAL-switch can be controlled by the availability of the "half-line pulse" being in proper phase. The demodulated signals (B–Y) are available at pin 7, the (R–Y)-signals can be picked up at pin 4 of the IC. An internal green-matrix generates the difference signal (G–Y) at pin 5. Three 150-μH-chokes, having a resonant frequency of twice the colour subcarrier frequency, eliminate remainders of the subcarrier signal at the colour-difference outputs. These remainders always have the double frequency when this principle of symmetrical demodulation is used. The output signal can be supplied either to the output-stage transistors–if a receiver with colour difference drive is used- or to the matrix stage–if a RGB-drive is maintained. The circuit is suitable for a concept, in which a black-level clamping in the following stage is provided. The temperature stabilization of the TAA 630 S is not sufficient for an inverse dc feedback. A coarse shifting of the dc level at the outputs is obtainable by varying the resistors R_{16} and R_{17}.

The coils L_{F1} to L_{F5} are available from the company Toko.

3.7 Mains separated power supply for colour TV-receivers

Mains separated power supplies offer a lot of advantages for the total concept of a colour TV receiver. The antenna can be coupled to the tuner directly and sockets for video, head phones as well as tape recorders can be incorporated to the set without any additional elaborateness.

The circuit of the power supply **(fig. 3.7)** operates upon the principle of a non-synchronized, self-oscillating dc converter. It oscillates with a frequency between 20 and 28 kHz. All output voltages are stabilized and thus open-loop-proof as well as short-circuit-proof. The mains supply voltage may vary between 180 and 265 V. Mains voltage fluctuations of ±20% are reduced to ±2% at the output. The hum voltage of about 18 V_{pp} at the input capacitor is decreased to a value of 0.2 V_{pp} at the 200-V-output. As against conventional circuits without mains separation the circuit including the separation requires only a minimum of additional elaborateness in components. The transformer has to be moulded to meet VDE-standards.

Description of functions

The mains voltage is rectified in a bridge circuit (4×C 1740) and smothed through an electrolytic capacitor of 400 μF. The BU 126 operates as switching transistor. The control of the output voltages is attained by affecting the energy which is stored in the transformer during the forward period.

A balance is achieved between the energy stored during the forward period and the one released during the reverse period. The stored energy is dosed by controlling the collector peak-current of the switching transistor BU 126.

In order to start the oscillation a starting pulse derived from the mains voltage is supplied to the base of BU 126.

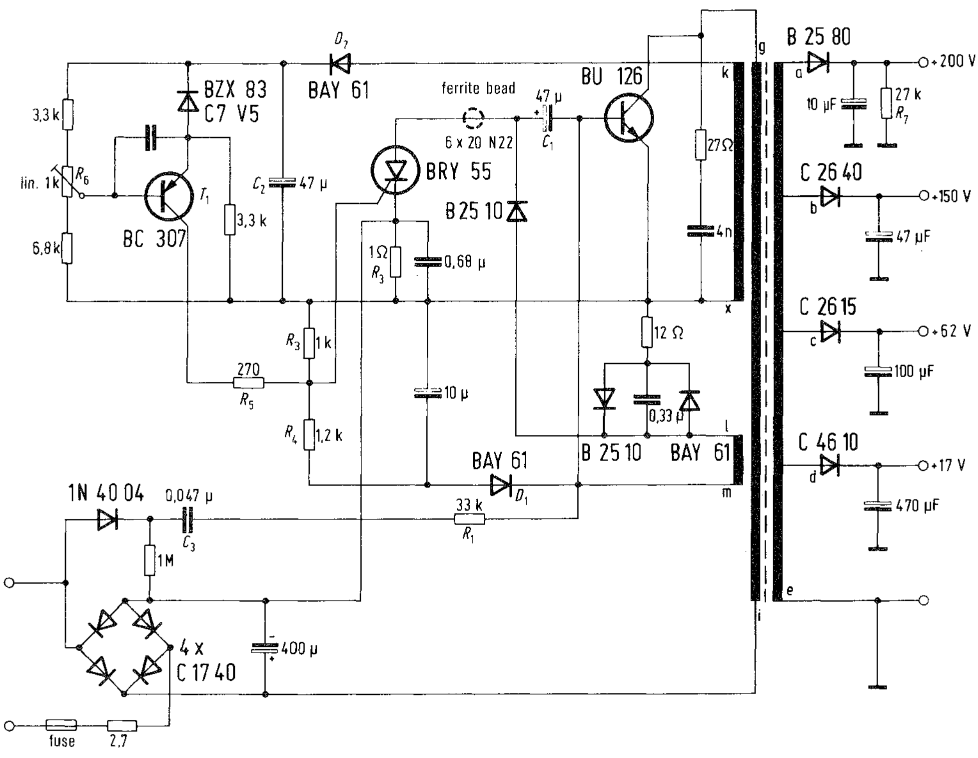


Fig. 3.7

Then the oscillation is maintained through the inverse-feedback winding l-m. Across the resistor R_2 drops a voltage which depends on the collector current of the BU 126. Through the voltage divider R_3/R_4 the gate of the switching-off thyristor BRY 55 is biased to a level of $-2\,V$ refered to the cathode. The negative voltage for the voltage divider is generated through the diode D_1

from the voltage across the feedback winding during the reverse period. The voltage drop across the resistor R_2 opposes now the negative bias of the gate. As soon as the triggering level (about +0.7 to 1 V) is exceeded, the thyristor fires. When the thyristor is switched a negative level is achieved at the base of the BU 126 by the capacitor C_1 and turns off the transistor. The thyristor remains conductive during the switching and reverse time of the BU 126 and it is turned off at the zero-axis crossing, which is achieved by the polarity change of the reverse-feedback voltage.

The max. possible collector peak-current of the BU 126 depends on the dimensioning of the voltage divider R_3/R_4. If the divider is not loaded the maximum is about 3 A. If it is loaded by the transistor T_1 and the resistor R_5 the negative bias is changed during the control process. If the bias is high the auxiliary thyristor triggers only at high collector peak-currents, i.e. much energy is stored in the transformer. In order to decrease the amount of stored energy the bias is reduced in a simple way by loading the voltage divider. The control information is generated from the winding k–x, which is tightly coupled to the windings of the output voltages. The diode D_2 generates a dc voltage which depends on the output voltage. The control transistor is turned on when the voltage at C_2 exceeds a fixed level adjusted by the potentiometer R_6. Through this transistor the negative bias at the gate of the BRY 55 is reduced. Therefore the thyristor triggers earlier and the transistor BU 126 turns off already at lower collector peak-currents.

Auxiliary circuit for the beginning of oscillation

Defined starting pulses of a 5-ms-duration are generated from the mains ac-voltage by means of the diode 1 N 4004 and the RC-circuit C_3/R_1. They are supplied to the base of the BU 126 and the transistor becomes conductive. Thus the oscillation is started.

Open-loop operation

The power supply is suited for power outputs up to about 200 W. Between open-loop operation and a load of 70 W the power supply runs in a 50-Hz-intermitting-operation.

If the load is less than 70 W the switching frequency rises. Its period time becomes shorter than the turn-off time of the thyristor.The thyristor remains turned on and the oscillation is interrupted. A new beginning of the oscillation is possible only with the next starting pulse. During the open-circuit operation a pulse train with spacings of 20 ms is generated. The resistor R_7 acts as basic load to prevent an extremely high increase of the output voltages. It has been practically experienced that thus a high softy is achieved at open-circuit operations.

Standard operation

The standard-operation ranges between 75 W and about 200-W-loads.

Short-circuit operation

If a short-circuit occurs at one of the outputs the self-oscillating dc converter changes to an intermitting operation. The continuous sequence of collector peak-current pulses is replaced by a pulse train with a spacing of 20 ms. This behaviour results from the 50-Hz-starting-circuit. At the same time the spacing of the individual current pulses is increased to about 2 ms (standard operation: 40–50 μs). Besides that the collector voltage of the BU 126 is reduced from about 600 V_{pp} to max. 380 V. The maximum ratings of the BU 126 are not exceeded during short-circuit operation. Special attention has to be paid to the output short-circuit current, if only one of the outputs has a short-circuit. This short-circuit current may not exceed the admissible diode current of the individual rectifiers. This is achieved through a special starting circuit. The short-circuit depends on the energy stored in the transformer. This energy can be minimized by decreasing the numbers of collector-current pulses pro time unit. First the collector peak-current of the BU 126 is increased when a short-circuit occurs. This, however, causes a firing of the thyristor and a turn-off of the BU 126. At the same time the voltage across the winding l–m is reduced and thereby the bias for the voltage divider R_3/R_4 is also decreased. Therefore the triggering level of the thyristor is achieved at lower collector currents.

The transistor can be switched only, when the thyristor is turned off and when a new starting pulse is available. Collector-current pulses are only possible during the defined starting period of 5 ms, which follows with a distance of 20 ms (50-Hz-mains frequency).

The described power supply is available as a module under the ordering code AZB 5000. However, the bridge-rectifiers and the charging capacitor are not included.

Mains voltage range	180 V to 265 V
Nominal output voltages	200 V = /0.1 A
	150 V = /0.8 A
	62 V = /0.25 A
	17 V = /1 A

3.8 Touch keys

(see chapter 7.5)

3.9 Multi-burst generator

For frequency response checks of video transmitting devices and of video recorders as well as for the alignment of the frequency response compensation in TV-cameras a so-called multi burst signal is preferably used. This signal contains a constant sequence of oscillation bunches with individual discrete frequencies, e.g., 1, 2, 3, 4 and 5 MHz. It is principally constructed like a video signal, i.e. it includes blanking intervals and synchronizing pulses. Because of this standard-like construction this signal is more favoured than continuous sweep signals, which may cause disturbances of the blanking stage, the clamping circuit and the sync.-pulse generators during the signal processing.

For transmitting systems mostly multi burst generators with sinusoidal oscillation bunches are used today. For checks of TV camera-amplifiers a rectangle-multi-burst generator seems to be more advantageous, since it supplies a signal which is analogous to the one of the bar pattern. Latter is used as a criterion for the resolution of TV cameras (depth of modulation). Is the camera amplifier checked with the rectangle-multi-burst generator according to an optimal picture the bar pattern is also reproduced in an optimal way.

Besides that the rectangle-multi-burst seems also to be applicable for other tests, since it is abvious that in actual TV-pictures sinusoidal signals are rarer than step-function signals and needle pulses.

Another advantage is the relatively simple circuit which is used to generate rectangle-multi burst signals. The multi-burst generator shown in **fig. 3.9.1** supplies 8 bars along a line. The first of it is a white bar, the other seven contain frequencies from 1 to 7 MHz **(fig. 3.9.2)**.

The clock pulses for the bars are generated by an astable multivibrator (9, 13), oscillating with a 10 times-line frequency (M_1). The line frequency is achieved through a decimal counter

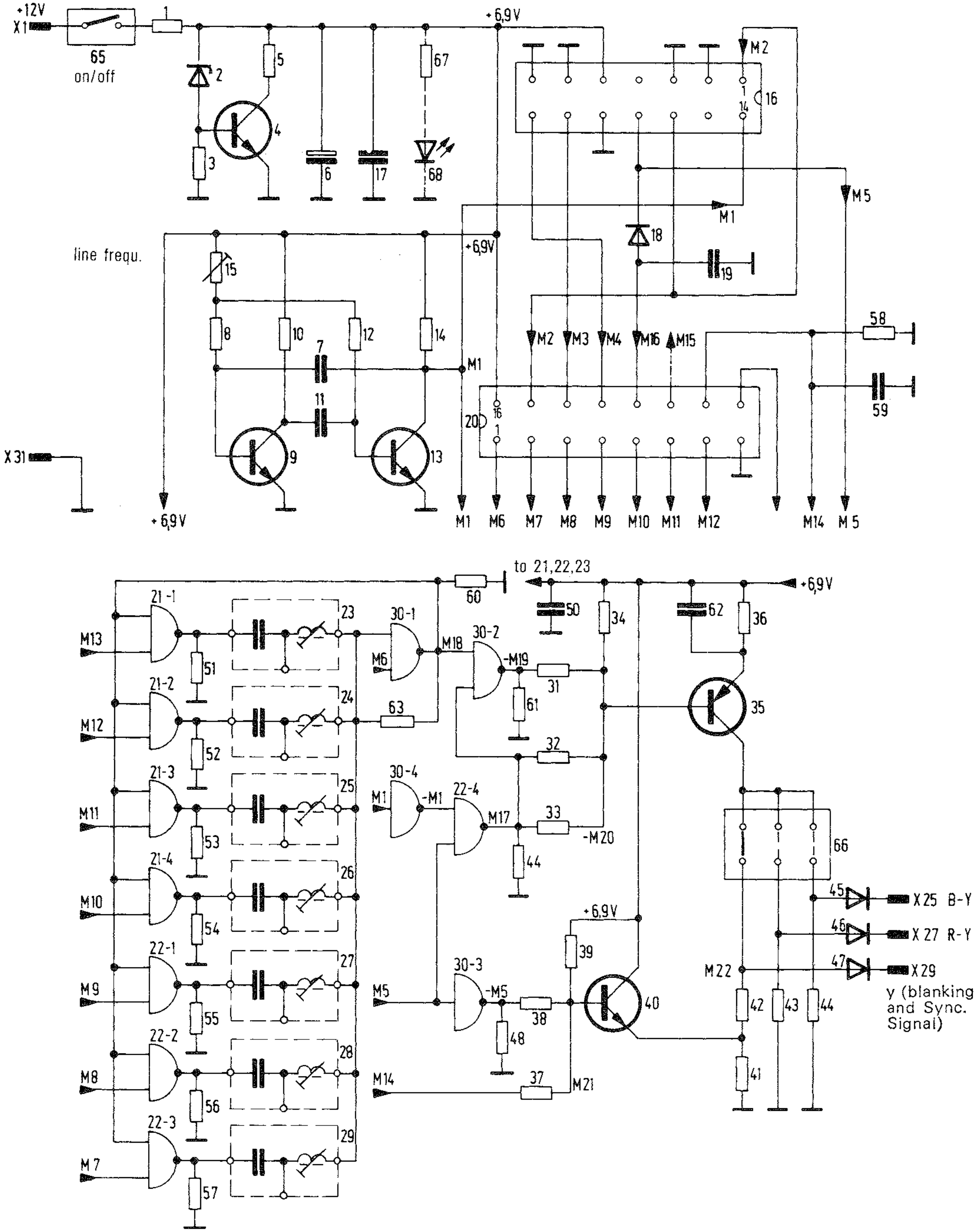

+12V
X1
65
on/off
+6,9V
line frequ.
X31
+6,9V
M1 M6 M7 M8 M9 M10 M11 M12 M14 M5
M2 M3 M4 M16 M15
to 21,22,23
+6,9V
M13
M12
M11
M10
M9
M8
M7
M18
-M19
-M1
M17
-M20
M5
-M5
M14
M21
M22
X25 B-Y
X27 R-Y
X29
y (blanking
and Sync.
Signal)

Fig. 3.9.1

FLJ 161 (16). The blanking pulses for the bars (M_6 to M_{13}) or the synchroneous pulses (M_{14}) are derived from the BCD-signals (M_2, M_3, M_4, M_5) of the counter by means of the decoder FLH 281 (20).

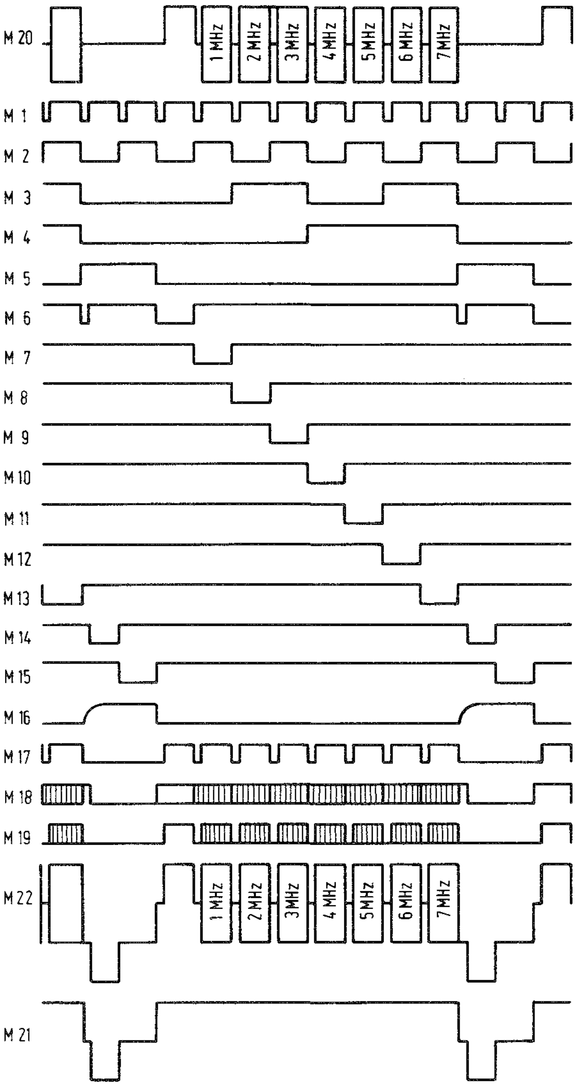


Fig. 3.9.2

To produce the front porch the leading edges of M_5 are delayed by D_{18}/C_{19}, thus M_{16} is generated.

The blanking pulses M_7 to M_{13} control a multiple-start-stop-oscillator, which contains the resonant circuits 23 to 29 in the feedback-loop. The circuits are switched on successively through the NOR-gates 21-1 to 4 and 22-1 to 3. The common connection of these circuits is fed to the gate 30-1, which acts as a Schmitt-trigger by incorporation of R_{63}. The white bar

(M_6) is also supplied to this gate. The output signal of 30-1 (M_{18}) is fed to the inputs of the selection gates and thus the feedback loop is closed.

The flyback blanking is obtained by M_5. There is an additional blanking with M_1 between each bar. The pulse duty factor is rated adequately. The blanking signal M_{17} of the multi-burst is generated by the gates 30-4 and 22-4. The blanking is achieved in the gate 30-2. To its output signal $-M_{19}$ the blanking pulses M_{17} are added in a resistor-matrix (31, 32, 33). Thus an ac voltage ($-M_{20}$) is produced.

In a second matrix (37, 38, 39) the synchroneous pulses M_{14} and the negative blanking pulses ($-M_5$) without bar-blanking are added in the way that a mixture M_{21} of the blanking and sync. signal is created with a blanking-signal content of 50%. This mixture is supplied continuously to the Y-output by the common-emitter circuit 40.

The blanked multi-burst-signal ($-M_{20}$) passes still the phase inverter 35 and it can be connected selectively to the Y-, (R-Y) or (B-Y)-output through the switch 66. If the Y-output is chosen, then the signal M_{22} is available at the terminal X_{29}, the signals at the colour-difference outputs are zero in this case. If one of the colour-difference outputs, however, is selected, the signal M_{20} is available at the output terminal and the signal M_{21} is supplied to the Y-output. Thus the synchronization of following devices (e.g. colour coder, monitor) is achieved in each mode of operation.

Vert.-pulses are not included to the supplied signal. Therefore monitors and VCR-units connected to the multi-burst generator operate with their natural picture frequency. But this does not influence the tests.

The supply voltage is 6.9 V and is achieved from +12 V by a stabilizing transistor circuit (T_4).

Dimensions

Length	L	160 mm
Width	W	100 mm
Height	H	30 mm

Terminals

X	31-pin plug
1	supply voltage +12 V
25	output B-Y
27	output R-Y
29	output Y, blanking and sync. signal
31	ground

Electrical characteristics

Supply voltage	$V_{X\,1}$	+12	V
Supply voltage tolerance	$V_{X\,1}/V_{X\,1}$	±10	%
Supply current	$I_{X\,1}$	about 400	mA[1])
Output Y, blanking and sync. signal	$V_{X\,29}$	1.4	V_{pp}[2])[3])
		0.9	V_{pp}[2])[4])
Output R-Y, B-Y	$V_{X\,27,\,25}$	1	V_{pp}[2])[4])
		0	V_{pp}[2])[4])
Internal impedance	$R_{X\,29,\,27,\,25}$	75	Ω
Line frequency	f_H	15625	Hz
Tolerance	$\Delta f/_H/f_H$	1	%
Sync. pulse duration	t_s	4.8	µs
horiz. blanking-time	$t_{h.\,b.}$	12.8	µs
Pulse rise-time	t_R	about 30	ns

Pulse fall-time	t_F	about 30	ns
Bar duration	t_B	4.4	μs
Separation of bars	t_A	2	μs
Bar sequence: 1	f_1	4.4	μs
2	f_2	1	MHz
3	f_3	2	MHz
4	f_4	3	MHz
5	f_5	4	MHz
6	f_6	5	MHz
7	f_7	6	MHz
8	f_8	7	MHz
Multi-burst frequency error	$\Delta f_X/f_X$	0.2	%

[1]) at V_{X1} = 13 V
[2]) at 75 Ohm
[3]) Multiburst supplied to Y-output by means of switch S 66
[4]) Multiburst supplied to (R-Y) or (B-Y)-output by means of switch S 66

List of parts

Item	Type	Value	
1	R	15 E/2 W	
2	D	BZY 85 6V2	
3	R	100 E	
4	T	BC 238	
5	R	39 E/2 W	
6	C	220 μ/10 V	
7	C	470 p/Styro	
8	R	10 k	
9	T	BC 238	
10	R	1 k	
11	C	470 p/Styro	
12	R	10 k	
13	T	BC 238	
14	R	1 k	
15	P	2.5 k horizontal, small	
16	IC	FLJ 161	
17	C	10 n MKH	
18	D	AA 118	
19	C	1 n Styro	
20	IC	FLH 281	
21	IC	FLH 191	
22	IC	FLH 191	
23	LC	22 p/23 μH/7 MHz	FZ 41-17
24	LC	27 p/27 μH/6 MHz	FZ 41-16
25	LC	33 p/32 μH/5 MHz	FZ 41-15
26	LC	32 p/40 μH/4 MHz	FZ 41-14
27	LC	56 p/53 μH/3 MHz	FZ 41-13
28	LC	82 p/80 μH/2 MHz	FZ 41-12
29	LC	150 p/160 μH/1 MHz	FZ 41-11
30	IC	FLH 101	
31	R	2.2 k	
32	R	4.7 k	
33	R	47 k	
34	R	2.2 k	

Item	Type	Value	
35	T	BC 308	
36	R	75 E	
37	R	5.6 k	
38	R	4.7 k	
39	R	1.5 k	
40	T	BC 238	
41	R	150 E	
42	R	75 E	
43	R	75 E	
44	R	75 E	
45	D	BAW 75	
46	D	BAW 75	
47	D	BAW 75	
48	R	470 E	
49	R	470 E	
50	C	10 n MKH	
51	R	470 E	
52	R	470 E	
53	R	470 E	
54	R	470 E	
55	R	470 E	
56	R	470 E	
57	R	470 E	
58	R	470 E	
59	C	470 p ceramic	
60	R	470 E	
61	R	470 E	
62	C	150 p Styro	
63	R	470 E	
64	–		
65	S	one-pole on-off switch	
66	S	one-pole, three switching positions, V42264-K1-A2	
67	–		
68	–		
69	–	31-pin plug	C42334-A55-A7
70	–	Printed board	FX 529
71	–		
72	–		
73	–		
74	–		
75	–		

3.10 Needle-pulse generator

Very sharp, positive pulses with a time duration of less than 20 ns can be produced by the needle-pulse generator described in the following **(fig. 3.10.1)**. The output level is TTL-compatible. The spectrum of these pulses is nearly constant up to 25 MHz and in combination with an analyzer it is particularly favoured for frequency-response tests. The 10-db-decrease occurs at 100 MHz only. According to the desired resolution the frequency can be chosen in 4 ranges from 50 Hz to 50 kHz. Besides that an externally generated needle pulse can be supplied to the input in order to form the output needle pulse. Instead of the needle pulses also the internal square-wave oscillation or the external signal, formed into a rectangular pulse, can be picked up at the output. For the shortest pulse duration (20 ns) the internal impedance is lower than 0.5 Ω. For longer durations the differential internal impedance is the same, the amplitude, however, is reduced, since the output current is limited with increasing loads.

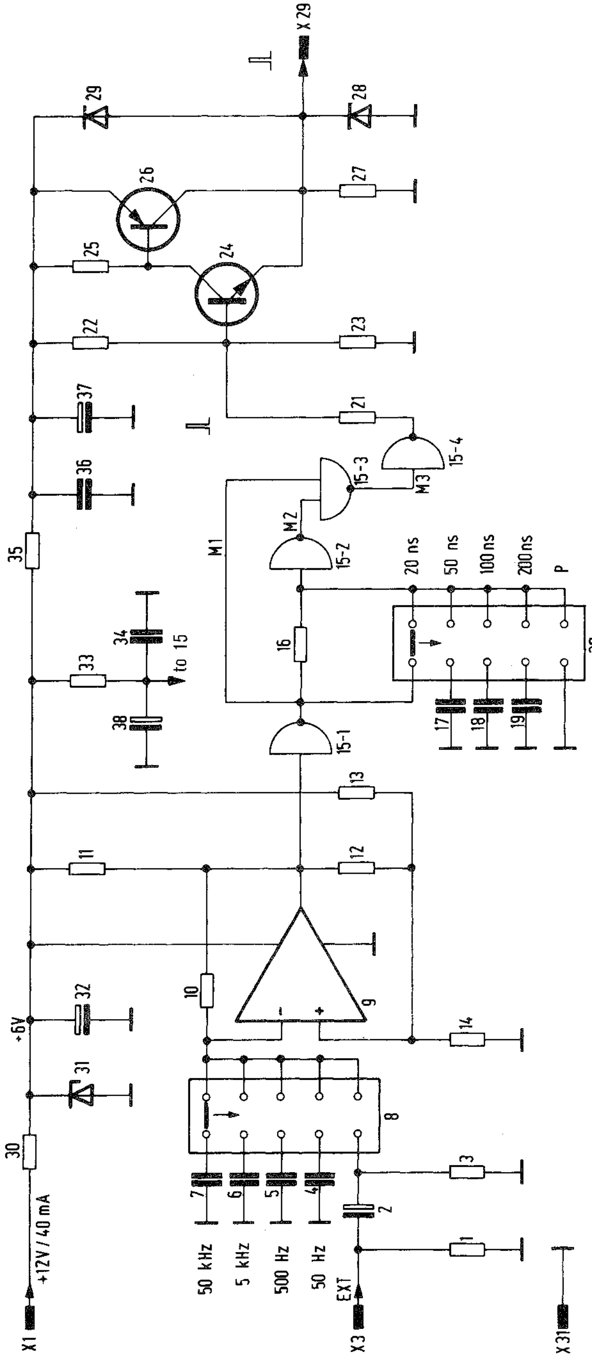


Fig. 3.10.1

The operational amplifier TAA 861 A (Pos. 9) operates as an rectangular pulse generator in the four upper switch positions, whereby the frequency is determined by the capacitors 4, 5, 6 and 7 **(fig. 3.10.2)**.

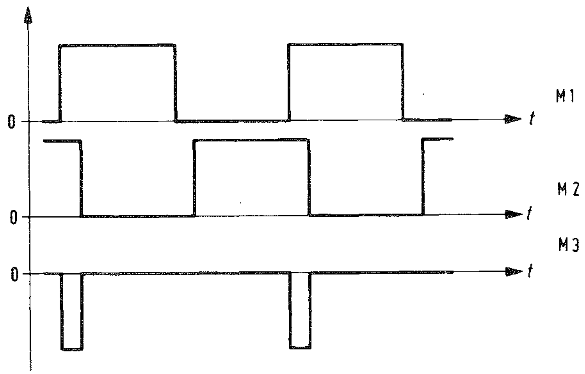


Fig. 3.10.2

The pulses are supplied to an inverter (15-1), which serves as a buffer. Its output is connected to a switchable delay circuit. The delay time can be selected by the four upper positions of the switch 20. After the delay circuit a second inverter 15-2 follows. Its propagation delay becomes effective in addition to the selected delay time. The signals available at the test points M_1 and M_2 are combined in the AND-gate 15-3. Its output supplies needle pulses (M_3) with a time duration that corresponds to the selected delay time. In the upper switch position the shortest pulse time-duration is achieved in accordance to the propagation time of the gate 15-2. Then the signal passes an additional inverter (15-4) and a low-resistive output amplifier. The output is protected through diodes (28, 29).

Instead of needle pulses also rectangular pulses can be generated, if the switch 20 is in its lower position. In this case the inverter input (15-2) is connected to a "low" level, the output M_2 becomes "high" and the pulses at M_1 pass continuously the gate 15-3.

In lieu of the internal rectangular oscillation, needle pulses can also be generated by using a pulse which is derived from an external signal supplied to the input X_3. This operation mode is selected with the lowest position of switch 8. In this case the IC 9 operates as a Schmitt-trigger.

Dimensions

Length×width×height	160×100×30 mm

Terminals

X	31-pin plug
1	supply voltage +12 V
3	input for external trigger pulse
29	output
31	ground

Electrical characteristics

Supply voltage	$V_{X\,1}$	+12	V
Supply current	$I_{X\,1}$	+40	mA
Ext. trigger voltage	$V_{X\,3}$	3	V_{pp}
Input impedance	$R_{X\,3}$	75	Ω
Output impedance (at 75 Ω)	$V_{X\,29}$	+3	V_p
Internal impedance ($t_{P\,1}$ = 20 ns)	$R_{X\,29}$	$\leq$0.5	Ω
Repetition frequencies	$f_{R\,1}$	50	Hz
	$f_{R\,2}$	500	Hz
	$f_{R\,3}$	5	kHz
	$f_{R\,4}$	50	kHz
Pulse duration	$t_{P\,1}$	20	ns
	$t_{P\,2}$	50	ns
	$t_{P\,3}$	100	ns
	$t_{P\,4}$	200	ns
	$t_{P\,5}$	$\frac{1}{2} f_R$	
Frequency stability	$\Delta f/f_R$	±5	%
Pulse-duration stability	$\Delta t/t_P$	±5	%

List of parts

Item	Type	Value
1	R	75 E
2	C	470 μ/3 V
3	R	10 k
4	C	1.5 μ MKH
5	C	150 n MKH
6	C	15 n MKH
7	C	1 n Styro
8	S	(5-pole change-over switch)
9	IC	TAA 861 A
10	R	10 k
11	R	1 k
12	R	4.7 k
13	R	4.7 k
14	R	4.7 k
15	IC	FLH 101
16	R	470 E
17	C	100 p Styro
18	C	220 p Styro
19	C	190 p Styro
20	S	(5-pole change-over switch)
21	R	75 E
22	R	470 E
23	R	470 E
24	T	BC 148
25	R	470 E
26	T	BC 158
27	R	100 E
28	D	BAW 75
29	D	BAW 75
30	R	150 E
31	D	BZY 55/C6V2
32	C	470 μ/6 V
33	R	10 E

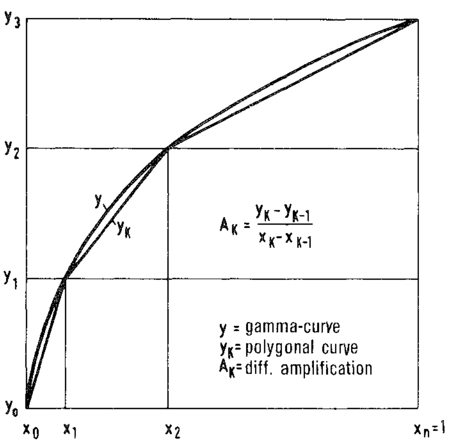
Item	Type	Value
34	C	100 n ceramic
35	R	10 E
36	C	100 n ceramic
37	C	100 μ/6.3 V
38	C	100 μ/6.3 V
39		
40		
41		
42		
43		
44		
45		
46		
47		
48		
49		
50		

3.11 Gamma-precorrection circuit

In TV cameras using recording tubes with a gamma of 1 it is generally necessary to establish a precorrection of the picture tube reproduction-curve. The picture tube has a gamma between 2 and 3.5. Thus the gamma of the precorrection characteristic has to range accordingly between about 0.3 and 0.5. In most cases it is sufficient to operate with a constant precorrection value of e.g. 4.

All methods of gamma corrections presume a non-linear characteristic, whereby an especially required curvature should be achieved definitely. This can be obtained approximately by using a polygon curve. The approximation of a gamma correction characteristic to a polygone curve is presented in **fig. 3.11.1**. There the output signal y of a non-linear network is shown as a function of the input signal x.

The output signal characteristic is subdivided in several sections. At the intersection points of both curves the fixed points for the polygon curve are determined.



K	y_K	$\gamma = 0.25$		$\gamma = 0.33$		$\gamma = 0.5$	
		x_K	A_K	x_K	A_K	x_K	A_K
0	0	0	–	0	–	0	–
1	0.33	0.01	33.3	0.04	8.34	0.11	3.3
2	0.66	0.20	1.75	0.30	1.28	0.44	1
3	1	1	0.42	1	0.48	1	0.59

Fig. 3.11.1

The table of **fig. 3.11.1** shows the results for various gamma values. The output signal is subdivided into three sections.

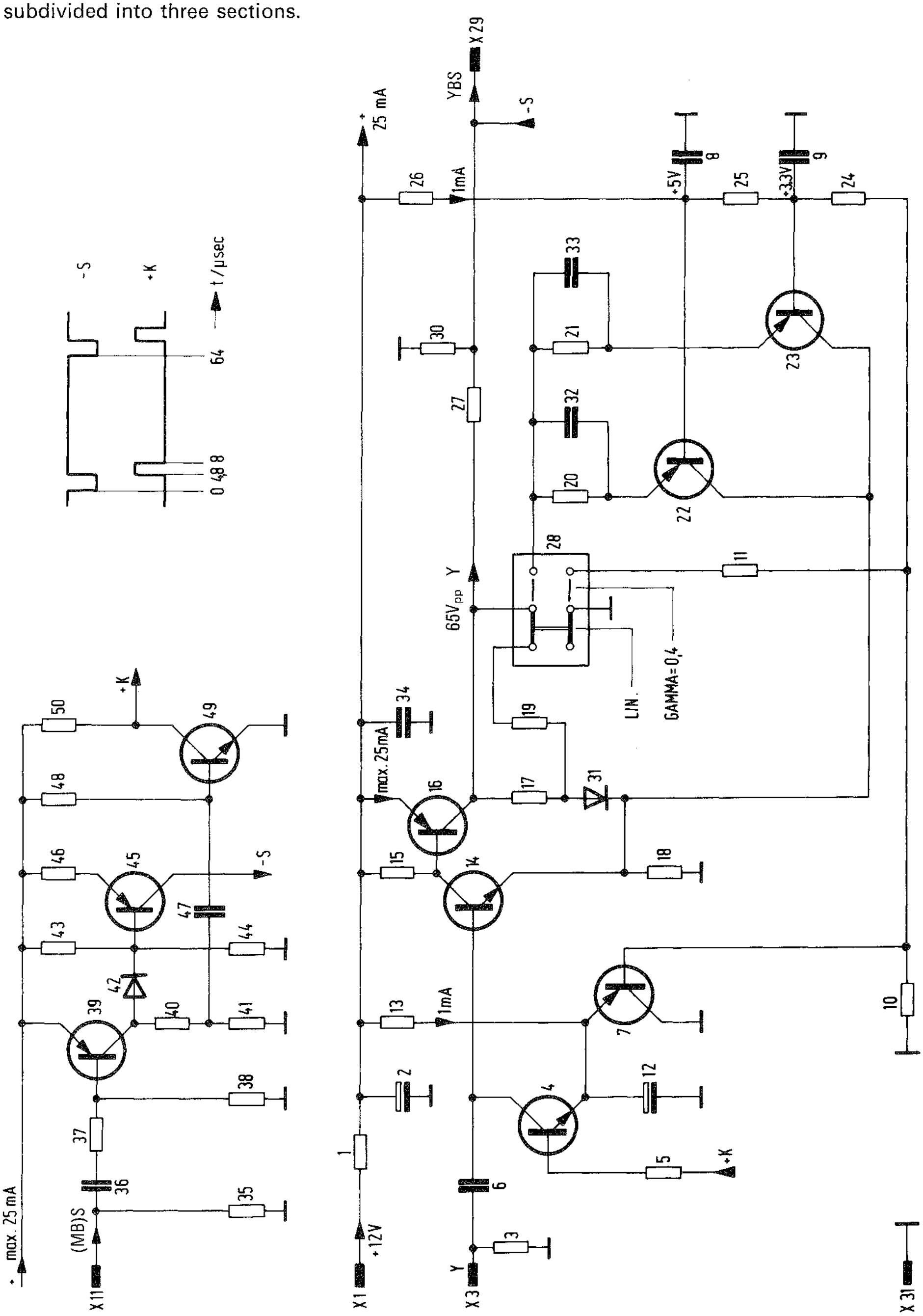


Fig. 3.11.2

The slope A_K of the different polygone curves corresponds to the required signal-amplification of the several sections. It is obvious, that for small gamma values very high amplifications are necessary in the first section.

The circuit shown in **fig. 3.11.2** achieves a fixed precorrection of a video signal with $\gamma = 0.4$. The distortion is obtained through a non-linear, reverse feedback, whereby the gamma characteristic is replaced by a polygon curve. The different end-points of the polygon curve correspond to threshold levels at which the gain of the video amplifier (14, 16) is changed by varying the reverse feedback. Two transistors (22, 23) operate as a threshold switch. A linear operation is also possible. In this case the threshold switch does not run and the linear reverse feedback is achieved by the resistor R_{19}.

As a relatively high gain is required in the first section of the polygon curve, attention has to be paid particularly to the black-level stability at the input of the amplifier. A blanked clamping circuit is used (T_4). The V_{BE}-temperature response of T_{14} is compensated by that of the transistor T_7, which supplies also the blanking level. The blanking signal and the switching one for the reverse feedback are taken from the same voltage divider (10, 24, 25, 26). Thus supply voltage fluctuations of ±10% do not result in harmful influences.

In order to optimize the switching from T_{22} to T_{23} the capacitors C_8 and C_9 have to be connected to their bases and such with small capacitances (32, 33) have to be placed in parallel to the emitter resistors (20, 21).

The diode 31 has the same temperature response as the base-emitter junction of T_{22} and T_{23}. Therefore temperature effects of the reverse feedback circuit are compensated.

The amplifier operates in such a way that the supplied synchronizing pulses are clipped. During linear operation the clipping circuit has to be set to a lower clamping value (switch 28).

A pulse processing circuit is provided for the generation of the clamping pulses +K and for the addition of new synchronizing pulses S at the output. The pulse separation circuit (39) splits the sync. pulses from a synchroneous or a multiplex blanked signal, supplied at terminal X_{11}. Through differentiation (47, 48) of the S-pulse leading edge and limitation (49, 50) positive clamping pulses are generated. They switch T_4 during the back porch.

Through an amplifier stage (45) the synchronizing pulses are added with a negative polarity to the video signal at the output of the gamma precorrection circuit. The diode D_{42} limits the sync. pulses, supplied to 45, and eliminates distortions during the line sweep.

Dimensions

Length×width×height	100×160×25 mm

Terminals

X	31-pin plug
1	supply voltage +12 V
3	input Y, blanked (S)
11	input (Y, blanked) S
29	output Y, b. and s. signal
31	ground

Electrical characteristics

Supply voltage	$V_{X\,1}$	+12	V
Supply current	$I_{X\,1}$	about 60	mA
Gamma		0.4	
Input Y, blanked (S)	$V_{X\,3}$	1 (1.4)	V_{pp}
Input (multiplex blanked) S	$V_{X\,11}$	0.4 (1.4)	V_{pp}
Input impedance	$R_{X\,3,\,11}$	75	Ω
Output Y, b. and s. signal	$V_{X\,29}$	1.4	V_{pp}
Output impedance	$R_{X\,29}$	75	Ω
Frequency response ±3 db up to	f_g	5	MHz

List of parts

Item	Type	Value
1	R	10 E
2	C	470 μ/12 V
3	R	75 E
4	T	BC 148
5	R	10 k
6	C	100 n ceramic
7	T	BC 158
8	C	100 n ceramic
9	C	100 n ceramic
10	R	120 E
11	R	120 E
12	C	100 μ/6 V
13	R	10 k
14	T	BC 148
15	R	1 k
16	T	BC 158
17	R	4.7 k
18	R	100 E
19	R	1.5 k
20	R	1 k
21	R	1 k
22	T	BC 158
23	T	BC 158
24	R	4.7 k
25	R	2.7 k
26	R	10 k
27	R	330 E
28		double-throw contacts
29	S	31-pin plug
30	R	100 E
31	D	BAW 75
32	C	22 p Styro
33	C	22 p Styro
34	C	100 n ceramic
35	R	75 E
36	C	100 n ceramic
37	R	100 E
38	R	220 k

Item	Type	Value
39	T	BC 158
40	R	420 E
41	R	470 E
42	D	BAW 75
43	R	3.9 k
44	R	6.8 k
45	T	BC 158
46	R	390 E
47	C	1 n Styro
48	R	10 k
49	T	BC 148
50	R	1 k

3.12 Digitizer

A television camera which is used only to pick up line-patterns is suitably equipped with a limiter in the video signal processing circuit. Such a limiter suppresses effectively noise influences. Independently of input signal variations an output signal with a fully utilized dynamic range is achieved, i. e. with a maximum black-to-white transition. In addition to that the edge steepness and thus the picture sharpness are improved.

The base of such a device is a standard camera with gray scale video signal (e. g. Siemens compact-camera). First of all an optimal compensation of the frequency response has to be aligned. If the compensation is wrong, the duration of needle pulses, for instance, is extended (lines of the picture pattern). The following limiter improves only edge steepness and pulse amplitude. Therefore a careful alignment is required.

The TTL-Schmitt-trigger FLH 351 is suggested as a limiter. **Fig. 3.12.1** shows a circuit of a so-called "digitizer", which is connected to the camera output. It supplies a binary video signal, which can be played back through a monitoring receiver.

The signal is amplified by T_{15} and T_{18} and supplied to the double-stage limiter. Since the sync. pulses are suppressed by the limiting, an additional sync. pulse separating circuit (T_{22} and T_{26}) is required. Its output supplies the synchronizing signal, which is mixed with the digitalized video signal in the output stage T_{32}.

The Schmitt-trigger is blanked by the synchronizing pulses to avoid unrequired influences.

The output of this device can also be switched to a linear operation. In this case the transistors T_{15} and T_{18} operate as buffer amplifier.

Thus the digitizer forms a linear video signal to a binary one. The output signal consists only of black-to-white transition signals, to which the sync. pulses are added. An improvement of the modulation depth and of the edge steepness is achievable, when line patterns and documents are picked up. The built-in Schmitt-trigger reacts to input signal variations having any slowness and supplies sharp output signal transitions. The threshold value is achieved at 50% of the white level.

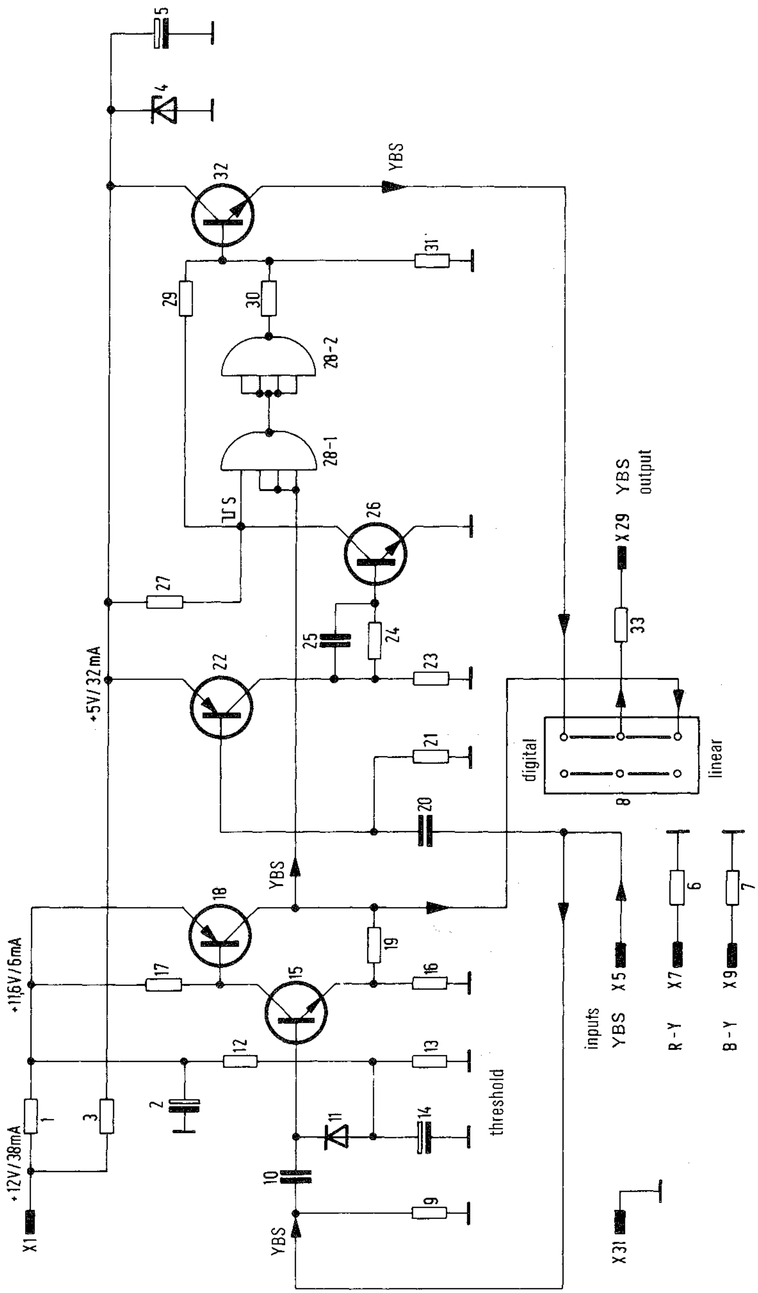

+12V/38mA
+11,6V/6mA
+5V/32mA
YBS
threshold
inputs
YBS
R-Y
B-Y
X1
X5
X7
X9
X29
X31
YBS
output
digital
linear
28-1
28-2

Fig. 3.12.1

Mechanical data

Height	H	30 mm
Width	W	100 mm
Length	L	160 mm
Weight	G	75 p

Terminals

X	31-pin plug
1	Supply voltage
3	Input YBS
5	(Input R–Y)
7	(Input B–Y)
29	Output YBS
31	Ground

Electrical characteristics

Supply voltage	$V_{X\,1}$	+12	V
Supply current	$I_{X\,1}$	38	mA
Input YBS	$V_{X\,3}$	1.4	V_{pp}
Input impedance YBS, R–Y, B–Y	$R_{X\,3,\,5,\,7}$	75	Ω
Output YBS	$V_{X\,29}$	1.4	V_{pp}
Output impedance	$R_{X\,29}$	75	Ω
Rise and fall time of output signal	T_{AF}	30	ns
Threshold[1])	V_s/V_{max}	50	%
TC of threshold[1])	V_s/V_{max}	0.2	% grd^{-1}

[1]) refered to the black-white step at the input (= 100%)

List of parts

Item	Type	Value
1	R	68 E
2	C	22 μ/12 V
3	R	220 E
4	D	BZX 55/C4V7
5	C	100 μ/6 V
6	R	75 E
7	R	75 E
8	S	2×throw-over
9	R	75 E
10	C	100 n
11	D	BAW 75
12	R	47 k
13	R	4.7 k
14	C	10 μ/3 V
15	T	BC 148
16	R	100 E
17	R	1 k
18	T	BC 158
19	R	100 E
20	C	100 n
21	R	100 k
22	T	BC 158

23	R	1 k
24	R	10 k
25	C	220 p ceramic
26	T	BC 148
27	R	1 k
28	IC	FLH 351
29	R	3.9 k
30	R	2.5 k
31	R	4.7 k
32	T	BC 148
33	R	75 E
34		31-pin plug
35		PC-board

4. Optoelectronic circuits

4.1 Automatic lamp control

In the following a circuit is shown using the photodiode BPW 33 (**fig. 4.1** and **4.1.1**). By this circuit it is possible to turn on a combination of 3 lamps very accurately in the suggested or inverse sequence, if three different illuminance threshold values have been set between 0.5 lx and 100 lx.

a: lamp 1
b: lamp (1+2)
c: lamp (1+3)

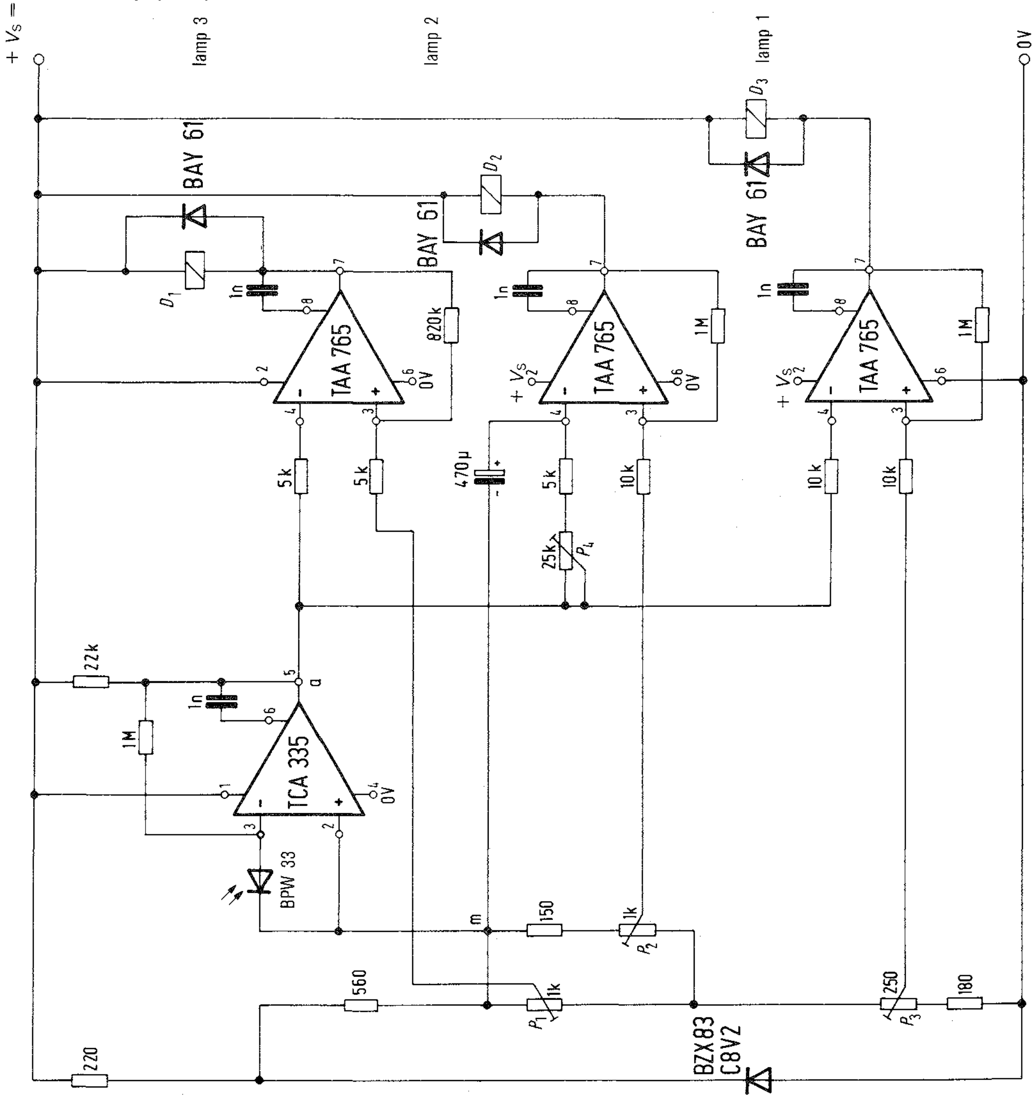


Fig. 4.1

The photodiode BPW 33 shorts the opamp TCA 335, operating as a linear amplifier, and thus controls three threshold switches. The output voltage of the TCA 335 changes as a function of illuminance. The lower limit is specified with 0.5 lx at an error of 0.1 lx, if a photodiode is used with a reverse current of less than 7 nA at $V_R = 10$.

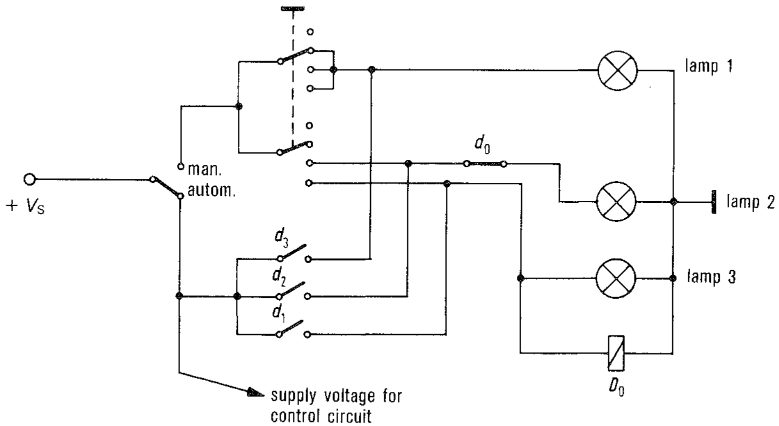


Fig. 4.1.1

The threshold-switch reference voltages, corresponding to fixed illuminances, can be adjusted by potentiometers and are regulated by a z-diode.

A delay circuit is additionally used for lamp 2 to prevent that lamp 1 and lamp 2 are switched permanently back and forth, if the illuminance changes rapidly and frequently. The delay depends on the adjustment of potentiometer P_4 and on the gradual illuminance change.

Voltage variations possibly occuring can be reduced by means of a filter circuit or a z-diode. Thus it is guaranteed that the reverse voltage of the TAA 765-output-transistor is not exceeded.

A max. current of 70 mA at 12 V is available at the output of the TAA 765. An additional driver transistor has to be connected to the output of the opamp, if relays requiring a higher current are to be used.

Technical characteristics

V_S	12 V
Temperature range	−20 °C to 60 °C
Adjustable range for lamp 1	70–100 lx
Adjustable range for lamp 2	10–70 lx
Adjustable range for lamp 3	0.5–70 lx
Current consumption without relays	25 mA
Relays D_1, D_2, D_3	>180 Ω

4.2 Linear Light-frequency-converter using BPX 48

To convert light of extremely high illuminance to a signal of relatively low frequency our photodiodes, combined with an astable multivibrator, are well suited **(fig. 4.2)**. The linear correlation between illuminance and clock frequency is achieved by the differential diode BPX 48, since

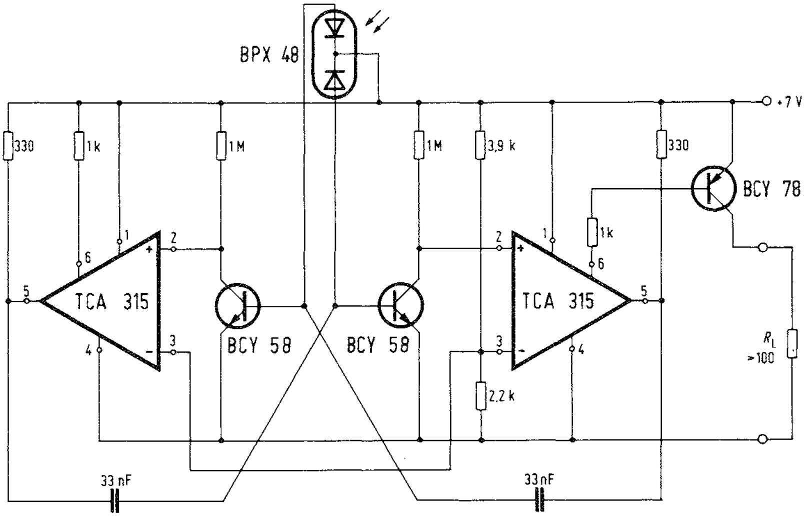


Fig. 4.2

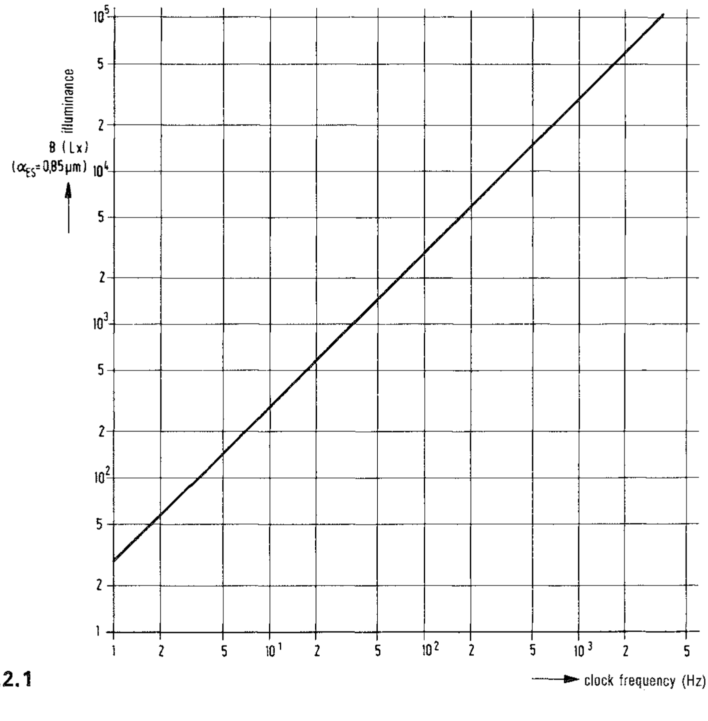


Fig. 4.2.1

its photocurrent can be impressed to both branches of the multivibrator in a wide range of illuminance. In order to reverse the charge of the capacitors determing the frequency as fast as required at a maximum of illuminance (250000 lx) the gain of the two multivibrator transistors is multiplied by one opamp each. The load is coupled to the multivibrator by an additional transistor. With the circuit shown in **fig. 4.2.1** a frequency variation of more than 1:50000 can be accomplished, i.e. in connection with a frequency counter a digital luxmeter without any range selector can be realized.

The upper clock frequency f_{ob} is achieved at the max. illuminance and is determined by the max. photocurrent, the capacitance and the operating voltage V_S.

It follows:

clock frequency $t = \dfrac{C \times V_S}{I_p}$ and

upper frequency $f_{ob} = \dfrac{I_{p\,max}}{2 \times C \times V_B}$.

Assuming that the supply voltage V_S is constant, the frequency can be adjusted by variation of the capacitors or by light attenuating filters.

The lower clock frequency, which is theoretically near zero, is determined mainly by the gain and the reverse current of the input transistors. According to these reasons the operating temperature should not be too high (e.g. less than 50 °C) and the reverse current I_{CBO} should not exceed its average value (for BCY 58 it is $I_{CBO} < 8$ nA at 50 °C). Under these conditions the described circuit operates unobjectionably up to a photocurrent of 80 nA. As the differential photodiode BPX 48 offers a photosensitivity of greater than 15 nA/lx the lower clock frequency occurs at about 5 lx.

The described circuit operates at photocurrents between I_p = 80 nA and 4.0 mA. These are supplied by the BPX 48 at illuminances between 5 and 250000 lx.

Electrical characteristics

Supply voltage		V_S = 7 V, constant
Supply current without R_L		$I_S \approx$ 25 mA
Frequency at	$I_p \approx$ 80 nA (= 5 lx)	$f \approx$ 0.18 Hz
	$I_p \approx$ 1 μA (= 65 lx)	$f \approx$ 2.3 Hz
	$I_p \approx$ 50 μA (= 3,300 lx)	$f \approx$ 115 Hz
	$I_p \approx$ 0.45 mA (= 30,000 lx)	$f \approx$ 1 kHz
	$I_p \approx$ 4 mA (= 250,000 lx)	$f \approx$ 9.5 kHz
Duty factor		1:1
Max. operating temperature		$T \approx$ 50 °C
Load		$R_L >$ 100 Ω

4.3 Logarithmic lux-meter with a silicon photodiode BPX 91

The following circuit was designed to detect illuminances (e.g. of an air conditioning plant). The illuminance is converted exponentially to a voltage (max. 400 mV to ground at 10^5 lx). The silicon photodiode BPX 91, acting as a sensor, operates on open circuit and supplies a logarithmic output voltage as a function of the illuminance. The transistor BCY 58 X amplifies the photocurrent and compensates also the TC of the photodiode by its base-emitter diode.

The desired output voltage as a function of the illuminance is available across the low-ohmic potentiometer P_2 driven by an opamp with a gain of 1. The circuit is to be adjusted as follows:

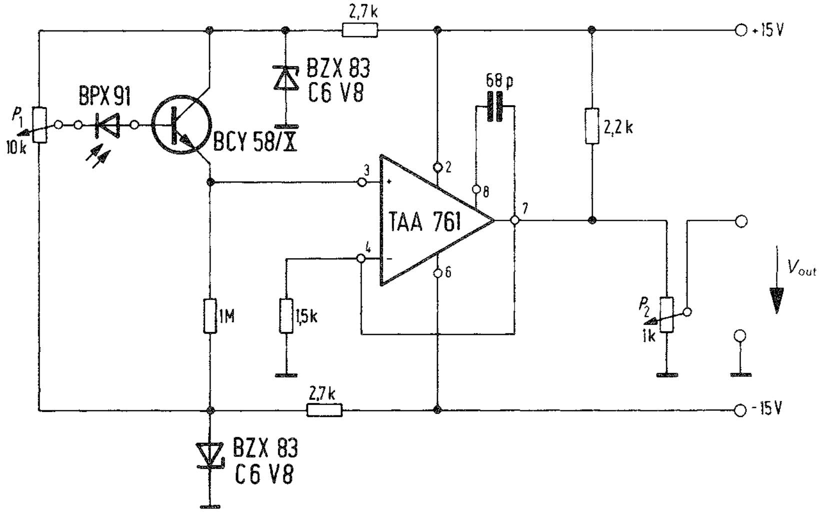


Fig. 4.3

1. Short the photodiode, adjust potentiometer P_1 as long as the output voltage V_{out} is zero.
2. Remove the short circuit, apply the max. illuminance to the photodiode, adjust the desired max. value of output voltage V_{out} (400 mV) by potentiometer P_2.

It has to be considered that the spectral sensitivity of the photodiode does not conform with the one of the human eye. Since the definition of the illuminance E (unit: lux) is refered to the sensitivity of the eye, the use of a correction filter is necessary infront of the photodiode, to get a real correlation between the value of the luxmeter and the voltage measured.

Technical characteristics

Supply voltage	±15 V
Supply current	about 15 mA
Output voltage at E = 10^5 lx (adjustable)	0 to 600 mV
Min. illuminance (with incandescent lamp)	
without filter	≈ 1.5 lx
with filter	≈ 15 lx

Correction filter BG 38, 2 mm thick (Company: Schott and Gen., Mainz)

4.4 Temperature coefficient elimination of LEDs

The radiation of light emitting diodes depends on temperature. This effect is disturbing at the most of applications and for its reduction or elimination a NTC-resistor can be connected in series with the diode. This compensation is, however, effective only over a small temperature range, because the TC of a NTC-resistor and the one of a LED differ in their temperature response. Therefore other different solutions have to be taken into consideration.

Curve a in **fig. 4.4** shows the relative luminous intensity I_L of a LED as a function of the ambient temperature ϑ_U at a forward current $I_F = 10$ mA. To reduce the temperature effect on the emitted radiation of a LED over a broad temperature range the circuit shown in **fig. 4.4.2** is particularly studied. The total current I_s is supplied from a 5 V constant-voltage source. The resistor R_p is connected in parallel to the LED.

The forward voltage V_F of the LED decreases with rising temperature (cf. **fig. 4.4**, curve b). Thus the current distribution in the circuit containing the LED and the shunt resistor R_p changes in favour of the LED. The total current I_s flowing in the circuit also rises. If the resistors R_v and R_p are optimally proportioned, the current flowing through the LED will increase with rising temperature to the same extent as its efficiency is reduced by the temperature coefficient. It is remarkable that this compensation remains practically constant over a broad temperature range.

Curve a in **fig. 4.4.1** represents the emitted radiation of a LED, type CQY 17, as a function of temperature when the temperature compensating circuit of **fig. 4.4.2** is provided. The photocurrent I_p of the detecting photodiode is a measure of the emitted radiation. Since the TC of this diode is much smaller than that of the LED, it has practically no effect on the measurement. The resistor R_v has a value of 41 Ω and the resistance of R_p is 13 Ω. The total current is I_s = 88 mA. Curve c **(fig. 4.4.1)** shows by way of comparison the emitted radiation of a LED, type CQY 17, used in a conventional circuit without parallel resistor R_p. The total current I_s is 10 mA and the forward current I_F flowing through the LED is in both cases 10 mA at an ambient temperature of ϑ_{amb} = 20 °C. It has to be considered that not only the LED but also the detecting photodiode (BPX 79) are exposed to the changing temperature.

Curve b and d in **fig. 4.4.1** show the test results of the same circuit configuration at a forward current of I_F = 5 mA. In this application the resistances are as follows R_v = 88 Ω and R_p = 27.5 Ω. The total current is I_s = 44 mA and 5 mA respectively.

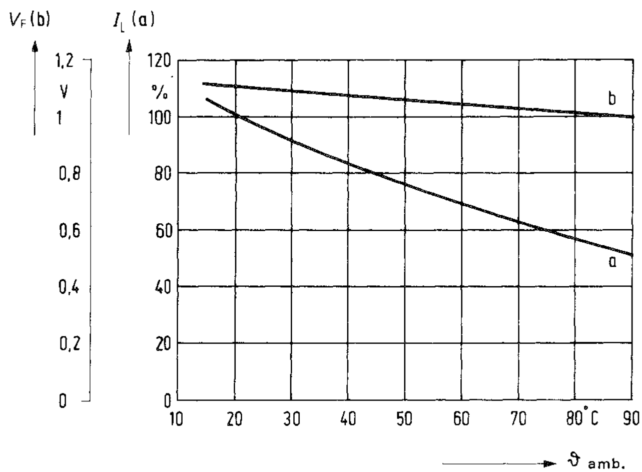


Fig. 4.4

The temperature compensating circuit can be used also for several LEDs simultaneously by connecting the diodes in series and shunting them with only one compensation resistor R_p **(fig. 4.4.2b)**.

The compensation of temperature effects for several diodes in common is more effective than that of only one. It has the advantage that the same results are realized for a parallel circuit with a lower total current. As a general rule, the lower the series resistance R_v, the lower is the total current required for compensation.

The temperature-effect compensation illustrated by the example of the LED CQY 17 is just as effective for other LEDs, especially for the types LD 261 to LD 269.

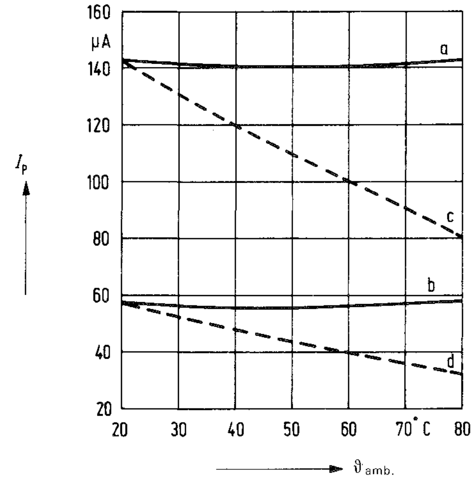


Fig. 4.4.1

a, b with compensation circuit (——)

a) I_F = 10 mA; I_s = 88 mA
R_v = 41 Ω; R_p = 13 Ω

b) I_F = 5 mA I_s = 44 mA
R_v = 88 Ω; R_p = 27.5 Ω

c, d without compensation circuit (– – –)

c) $I_F = I_s$ = 10 mA
d) $I_F = I_s$ = 5 mA

I_F, I_s at ϑ_{amb} = 20 °C

a one LED
b three LEDs in series
Rv series resistor
Rp parallel resistor
I_s total current
I_F diode forward current

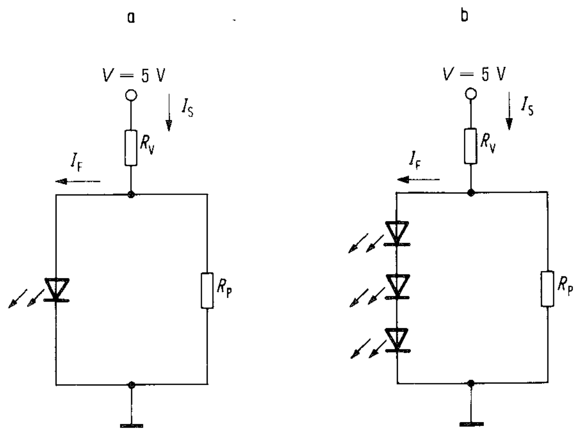


Fig. 4.4.2

4.5 Reducing the time constant of phototransistors

Signal rise as well as fall times of high sensitive phototransistors are relatively long, i.e. of the order of several microseconds. They can be reduced, however, to less than 0.5 μs by using an additional transistor connected between phototransistor and load resistor or to less than 0.1 μs by overcompensating the collector-base capacitance of the phototransistor.

In general phototransistors are much more sensitive than photodiodes or photovoltaic cells and as against avalanche photodiodes they have the advantage that they can be operated with a lower supply voltage with no great demands made as to its stability.

In conventional circuits with phototransistors, either the collector or the emitter is driven via a resistor and its voltage drop is used as output signal. In combination with an additional transistor the phototransistor can be operated as a Darlington amplifier. Although such Darlington circuits offer a high photosensitivity the rise and fall times are much longer than those of single phototransistors.

In the following two simple circuits, assuring high photosensitivity as well as short signal rise and fall times, are described.

Rise and fall times, t_r and t_f

By thorough tests it has been experienced that the fall and rise times of a phototransistor follow the relation

$$t_r,\ t_f = \sqrt{\frac{\beta^2}{4 \times f_T^2} + 4.8 \times \beta^2 \times C_{CB}^2 \times R_L^2},$$

where β denotes the current gain of the phototransistor, f_T its current gain bandwidth product, C_{CB} the collector-base capacitance, R_L the load resistance, t_r the rise time from 10% to 90% of the final value and t_f the fall time from 90% to 10%.

It should be considered that the characteristics β as well as f_T depend on the current, and C_{CB} on the voltage. Under conditions of a large signal operation the resulting rise and fall times are accordingly determined by integrating the successive sections of the phototransistor's characteristic. A typical phototransistor is the BPY 62. When no base current is supplied (no collector current without illumination) the signal rise and fall times are 8 μs each, whereat the load resistor R_L has a value of 1 kΩ and the collector current produced by illumination is 1 mA.

If a direct current is applied to the base of the phototransistor via a resistor, an operating point with higher transition frequency can be selected. At a collector dark current of 1 mA the signal rise time of the BPY 62 is about 6 μs.

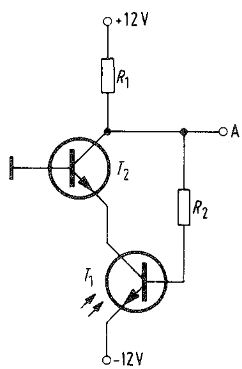


Fig. 4.5

Table 1: Rise time t_r, fall time t_f and photosensitivity $\Delta V/\Delta B$ of the circuit shown in **fig. 4.5**.

R_1 kΩ	R_2 MΩ	t_r, t_f μs	$\Delta V/\Delta B$ V/lx
1	1	0.5	2×10^{-3}
6.8	6.8	0.7	1.4×10^{-2}
10	10	2	2×10^{-2}
100	100	8	1×10^{-1}

Shortening the rise and fall times t_r and t_f

(t_r and t_f about 0.5 μs)

Fig. 4.5 shows a circuit with which it is possible to exceed the limit given by the above mentioned equation. The incident light causes a change in the collector current of the phototransistor T_1. At terminal A the output signal is achieved (refered to ground). Unlike in conventional circuits the collector of T_1 is not coupled directly to the load resistor R_1, but an additional transistor T_2 operated in a common base circuit is connected between the collector of T_1 and the resistor R_1. Thereby the small differential diffusion resistance RD of transistor T_2 takes effect at the collector of T_1.

The load resistance R_1 can be chosen relatively high; its value is only limited by the wiring capacity, being in parallel to terminal A. Thus the circuit shown in **fig. 4.5** supplies a far higher output voltage.

The operating point of the phototransistor is shifted in a section of the characteristic with high transition frequency f_T. For this reason a resistor R_2 is connected between the collector of transistor T_2 and the base of phototransistor T_1 to cause ac and dc feedback. The ac feedback shortens the signal rise and fall times still further and also reduces the influence of the transistor parameters on the signal edge steepness. The dc feedback reduces the influence of any dc gain tolerances of the phototransistor on the dark current. If BPY 62 is used for T_1 and BC 107 for T_2, signal rise and fall times of less than 0.5 μs will be attained with R_1 = 1 kΩ and R_2 = 1 MΩ. If the resistance of R_1 is raised to 6.8 kΩ and that of R_2 to 6.8 MΩ, the amplitude of the output signal will be six times as high, whereas the rise and fall times will remain below 0.7 μs.

The performance of the circuit shown in **fig. 4.5.1** is superior to that of the one shown in **fig. 4.5**. The added transistor operates as a phase inverter: the signal voltage u_K across the load resistor R_3 is in phase opposition to the one across the resistor R_1, thus driving the base of transistor T_2. By choosing an appropriate resistance of R_3 it is possible to realize that the signal voltage fluctuation caused by the signal current i_C at the collector of phototransistor T_1 becomes zero. If the signal voltage at the base of transistor T_2 is increased, the signal rise time is reduced still further because the reactive current flowing via the collector-base capacity of phototransistor T_1 is now overcompensated and thus turning the capacitance formally to a negative value. This negative capacitance is subtracted from the base-emitter capacitance of the phototransistor, whereby rising the cut off frequency. The limit of overcompensation is given by the self-excitation which occurs when the transmission factor of the circuit consisting of transistors T_2 and T_3 becomes greater than 1. In this case the phototransistor T_1 operates as an emitter resistor for transistor T_2. The larger the resulting collector output resistance of the phototransistor, the lower is the aforementioned circuit gain. Thus shorter signal rise and fall times can be realized without the occurrence of self-oscillation. If BPY 62 is chosen for T_1, BC 107 for T_2 and BC 177 for T_3, the signal rise and fall times will be shorter than 0.1 μs at resistances of R_1 = 1 kΩ, R_2 = 1 MΩ, R_3 = 20 Ω and R_4 = 390 Ω. Under these conditions there is no danger of self-oscillation.

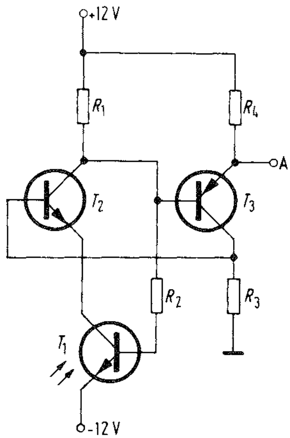


Fig. 4.5.1

Table 2: Rise time t_r, fall time t_f and photosensitivity $\Delta V/\Delta B$ of the circuit shown in **fig. 4.5.1**

R_1 kΩ	R_2 MΩ	R_3 Ω	R_4 Ω	t_r, t_f μs	$\Delta V/\Delta B$ V/lx
1	1	30	390	0.1	2×10^{-3}
6.8	6.8	20	390	0.25	1.4×10^{-2}
10	10	10	390	0.4	2×10^{-2}
100	100	150	3900	3	1×10^{-1}

4.6 Triac triggering with ac voltage phototransistors

Phototransistors are used as detectors for many applications, e.g. for light control systems, twilight switches, alarm systems, light barriers, positioning devices and position indicators. The motors, lamps or alarm devices of simple systems are particularly driven by ac. In this case novel phototransistors, operating also at a.c. voltage, offer considerable advantages. They are described in the following. Besides that it is possible to design circuits, which cannot be realized by the known phototransistors. One of the new phototransistors can also be used as a Darlington phototransistor.

In the circuit shown in **fig. 4.6** the current flow angle of triac T_1 is controlled in dependence on the incident light. The ac supply voltage is available between the terminals A and B. The load-in this case a lamp–is controlled by the series triac. The control of the current flow angle is achieved by a commonly known circuit. It consists of the resistor R_4, the triggering capacitor C_1 and the triggering device T_2. But the novelty of this circuit is the fact, that the abovementioned ac phototransistor is connected in parallel to the triggering capacitor. The more it is illuminated, the more is the charge flowing via the capacitor, i. e. the later the triggering voltage of the triggering device T_2 is reached by the voltage across the capacitor C_1. The current flow time of the triac is accordingly shorter and the power turnover of the load is lower.

If the load consists of a lamp which illuminates the ac phototransistor, then this arrangement is a simple light control device. But other control circuits can also be realized; e.g., positioning devices, where the illuminance applied to the ac phototransistor depends on the position of a light source, of a gap or of something else. If in these cases the load is an electromotor, for instance, a symmetrical characteristic of the phototransistor is very important for both polarities of the supplied ac voltage. Otherwise the current flow angle will be different for the two half-waves, i.e. an undesired dc current will flow through the ac motor. In comparison to photoresistors the ac phototransistor offers the advantage that it reacts with negligible inertia. Therefore control circuits with high gains can be applied without fear of self-oscillation.

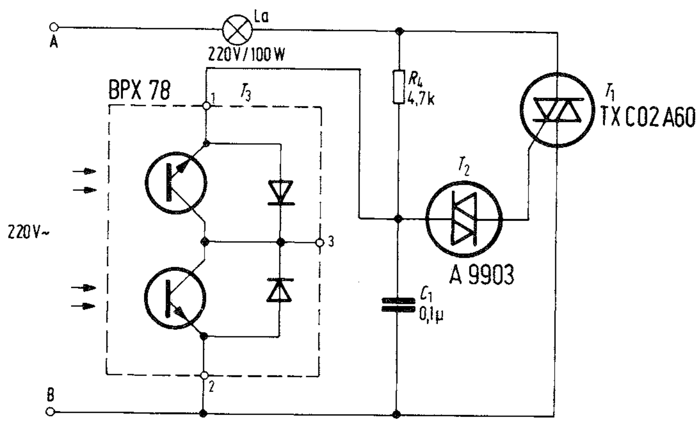


Fig. 4.6

4.7 Computer photoflash units with fast thyristors

The computer photoflash unit shown in **fig. 4.7** controls automatically the duration of the flash, i.e. the exposure is always correct regardless whether it is a close-up or a long shot, a bright scene or a dark one. For this purpose the light reflected by a photographed object is detected by a phototransistor and the suitable flash duration is derived adequately. In dependence on the reflected quantity of light the flash is interrupted sooner or later.

In the modern photoflash devices the connection between flash capacitor and flash tube is closed and interrupted by a thyristor, the so-called switching thyristor.

To turn off a thyristor a second one is required. This so-called turn-off thyristor is triggered at the exact time–in accordance to the reflected quantity of light.

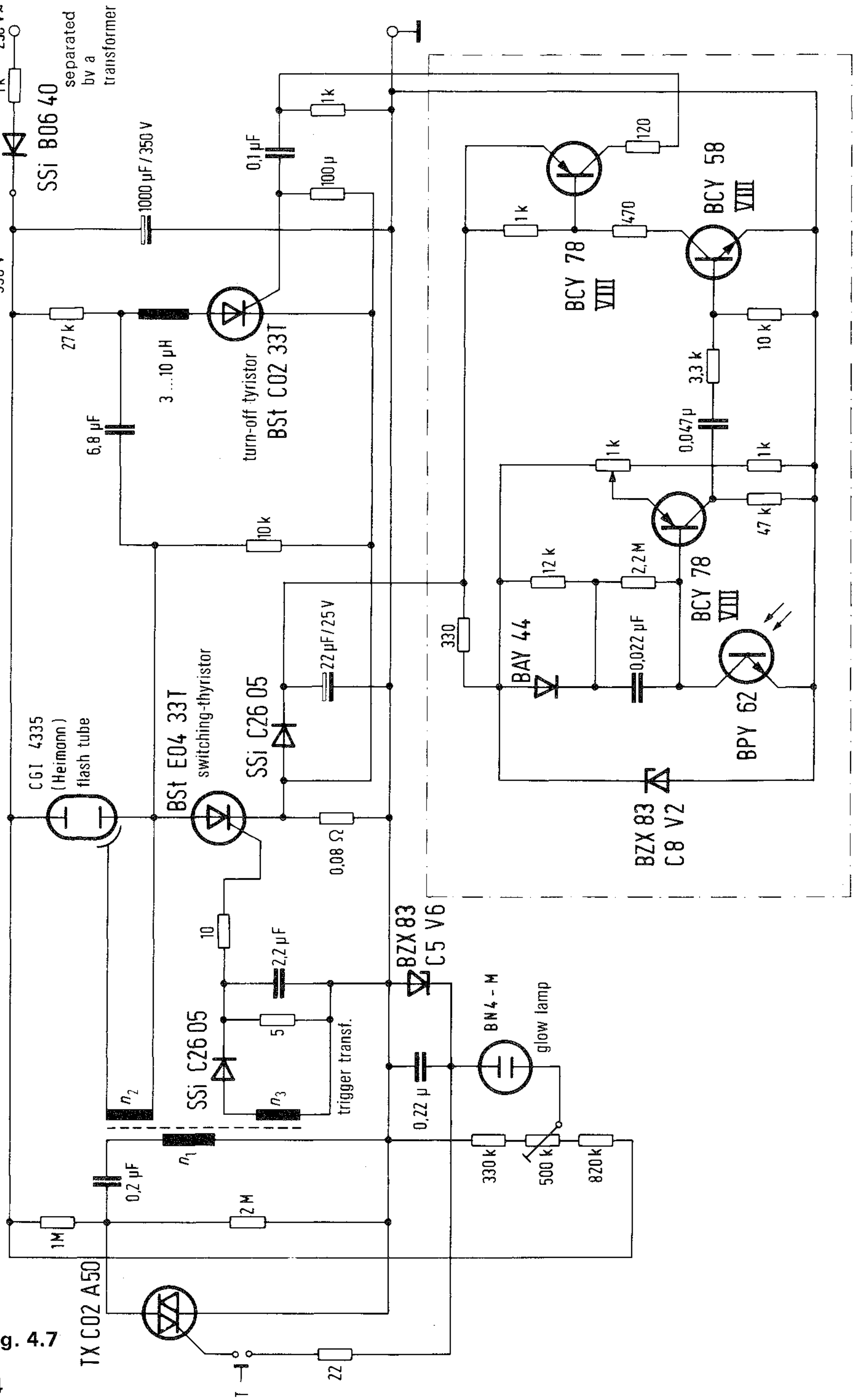

250 V~
1k
separated by a transformer
SSi B06 40
1000 µF / 350 V
350 V -
27 k
3 ... 10 µH
6,8 µF
turn-off tyristor
BSt C02 33T
0,1 µF
1k
100 µ
10 k
120
1 k
470
BCY 78
VIII
BCY 58
VIII
10 k
3,3 k
0,047 µ
1 k
1 k
47 k
BCY 78
VIII
12 k
2,2 M
330
BAY 44
0,022 µF
BPY 62
BZX 83
C8 V2
22 µF / 25 V
SSi C26 05
CGI 4335
(Heimann)
flash tube
BSt E04 33T
switching-thyristor
0,08 Ω
10
2,2 µF
BZX 83
C5 V6
5
SSi C26 05
trigger transf.
n_2
n_3
n_1
BN 4 - M
glow lamp
0,22 µ
330 k
500 k
820 k
0,2 µF
2 M
1M
TX C02 A50
22
T

Fig. 4.7

The correlation between the light quantity, picked up by the phototransistor, and the flash duration is achieved in a special circuit of the photoflash device, the so-called "computer" (framed by dashed lines in the schematic).

In the described device a triac is used for generating the triggering pulse in order to achieve a reliable contact connection when flash tube and switching thyristor are fired and to protect the thin contacts of the camera. The triac supplies a pulse with always the same duration even if the contact is closed slowly. The flash tube is fired through the trigger transformer in conventional manner. At the same time the switching thyristor is also turned on by a positive pulse supplied to the gate.

When the flash tube starts to emit light, a flash current of max. 250 A flows and generates a voltage drop of about 20 V across the 80-mΩ-cathode-resistor of the switching thyristor. This voltage is used as supply voltage for the computer. The phototransistor of the computer effects as a light-dependent resistor. Therefore the 0.022 μF-capacitor is differently fast charged or discharged in accordance to the quantity of light being supplied to the phototransistor. When the voltage across this capacitor, i.e. at the base of the transistor BCY 78, exceeds a certain, negative value as against the (adjustable) voltage of the emitter, the transistor becomes conductive. A positive surge is produced across the collector resistor of 47 kΩ. This surge is amplified and triggers the turn-off thyristor.

A turn-off capacitor of 6.8 μF serves as energy source for the turn-off thyristor. It is discharged through the turn-off thyristor and the switching thyristor, whereby in the latter the current flows in opposite direction as the flash current. Even if for a short moment only the turn-off current is higher than the flash current, the switching thyristor becomes not conductive and the flash is cut off. The energy remaining in the flash capacitor is not lost (as with conventional computer photoflash devices), but can be utilized for the following flash. By this method the electrical energy, supplied from small batteries or accumulators, is economically converted to light energy.

These are the most important components of the computer photoflash device:

1. Switching thyristor:	BStE 0433T	or BStE 0333T
2. Turn-off thyristor:	BStC 0233T	or BStC 0733T
3. Triac:	TXC 02A50	or TXC 03A50
4. Phototransistor:	BPY 62	or BP 101
5. Flash capacitor:	B43405-S0108-Q54, capacitance-constant	
6. Turn-off capacitor:	MKL 6.8 μF/250 V, B32110 E	
7. Fast diodes:	SSi C 2605.	

4.8 Operation of liquid cristal displays

The following circuits are particularly favoured for applications of liquid cristal displays, which operate accordingly to the principle of dynamic scattering. But they can also be used for the so-called fieldeffect displays. In this case, however, certain changes have to be made (especially reduction of the voltage levels).

Principle of operation.

In order to achieve a long life-time the LCDs have to be operated only at ac voltage. Already a dc content of less than 10% of the effective ac voltage effects a remarkable reduction of the life-time.

The frequency of the ac supply voltage should range between 30 and 150 Hz. At too low frequencies a flickering occurs and at higher frequencies the contrast is reduced. A frequency of

50 Hz has been proved well as a standard one. The shape of the ac voltage is without any influence. Therefore LCDs can be operated with, e.g., square-wave or sinusoidal voltages. The time mean value of the voltage amount determines the contrast. The application of square-wave voltages offers the advantage that a certain contrast is achieved with the lowest peak voltage.

As demonstrated in the following figures, the control of LCDs can be confined essentially to two methods.

The **figs. 4.8.1** and **4.8.2** show the so-called switching-method. Only one ac voltage is supplied either to the common electrode **(fig. 4.8.1)** or to the segments **(fig. 4.8.2)**. By means of a switch S either the current path is interrupted or the voltage source is shorted.

In the case of **fig. 4.8.1** it might be necessary to connect high-ohmic resistors (R') in parallel to the LCD-segments. This measure is especially required when capacitive or resistive leakage currents still can flow via the switch S even in its turned-off position.

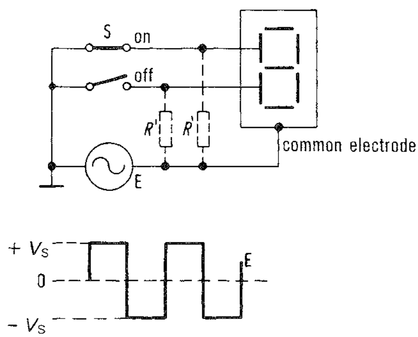


Fig. 4.8.1

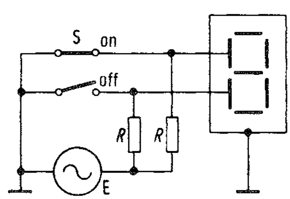


Fig. 4.8.2

The level of the used ac voltage is about 50 V_{pp} typical. **Fig. 4.8.3** shows the phase-shift method, which includes also two variations. It is characterized by the fact, that ac voltages of the same level and frequency are supplied as well to the common electrode (rear) as to the segments. The phase, however, can be different, i.e. either in phase or in phase opposition. Each amplitude of these partial voltages is only half the value of those shown in **fig. 4.8.1**. The phase-shift method is especially favoured if the reference voltage of the segments is less than 30 V, as it is required for MOS-circuits, for instance.

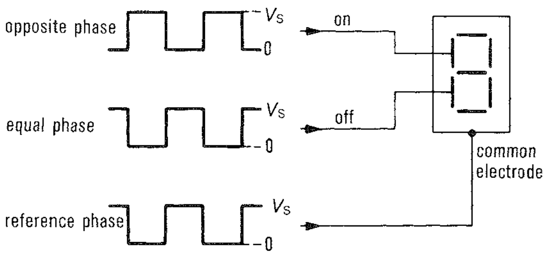


Fig. 4.8.3

In **fig. 4.8.3** it is shown that a voltage is impressed always to the segments. If this voltage is in antiphase to the one of the common electrode, the segment is energized; if the voltage is in phase, it is not energized, since no voltage is applied to the segment.

With the method shown in **fig. 4.8.4** the voltage is impressed to the segments only during the energizing. During the non-energizing period the segments are separated from the voltage source. To avoid undesired energizing, caused by leakage currents, resistors R′ have to be connected in parallel to the segments, as it is already demonstrated in **fig. 4.8.1**.

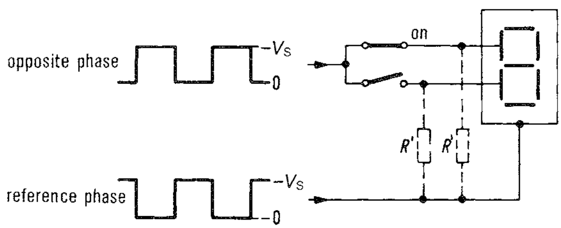
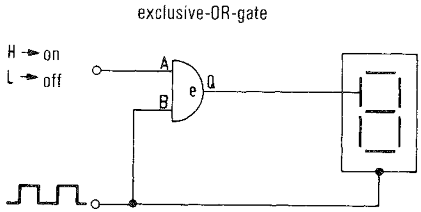


Fig. 4.8.4

A blocking capacitor with reasonably high capacitance is inserted in the lead to the common electrode to avoid safely unrequired influences of dc voltage contents (or also dc contents- these show the same results because V depends directly on I). But it has to be checked whether the charging of this capacitor causes too high voltage levels, which might create problems especially when MOS-circuits are used. The ac voltage phase shift by 180°, required at the phase-shift method, is achieved by a so-called exclusive-OR-gate. The principle of operation is shown in **fig. 4.8.5**. If L-level is applied to the input A, the ac voltage supplied to input B is available with the same phase at output Q. If, however, a H-level is applied to input A, the voltage phase at the output Q is shifted by 180° in accordance to the one of the voltage, supplied to input B. Thus it is possible to generate a voltage which is in phase or in opposite phase to the originally supplied one. The table of **fig. 4.8.5** demonstrates the logic functions once more.



logic functions
of the excl.-OR-gate

inputs		out
A	B	Q
L	L	L
L	H	H
H	L	H
H	H	L

Fig. 4.8.5

4.9 Design examples of LCD-single-segment control

Single-segment control means in this case that each segment has its own, individual lead-contrary to the matrix-control operation.

Mechanical switches.

Often it is possible to realize a simple and economical control device just with mechanical switches. As an example the switching matrix for the control of a 7-segment display, type AN 1301 is shown in **fig. 4.9.1**. The circuit is connected via a voltage divider directly to the 220-V-mains. No more than two DT contacts for each button are required to present the 10 digits.

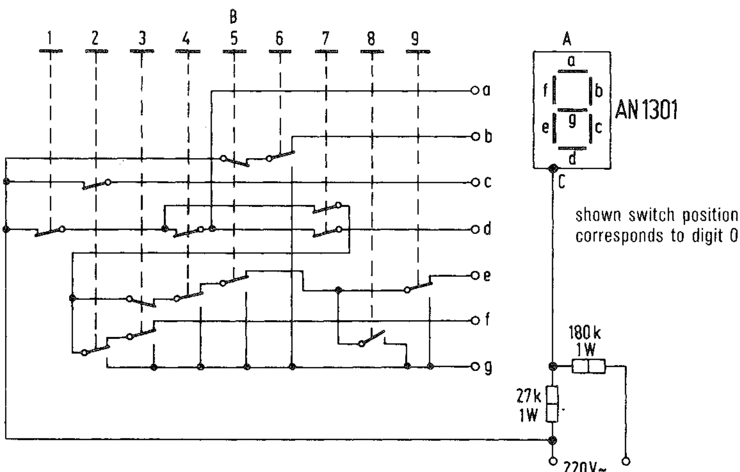


Fig. 4.9.1

Switch with bipolar transistors.

To replace a bidirectional switch two bipolar transistors are required, since as well the positive as the negative half-wave of the segment ac voltage have to be processed. **Fig. 4.9.2** shows a possible configuration for the operation of a 7-segment display by means of a comercial TTL-decoder (FLH 551). During the active state a H-level is available at the output of the decoder. Thus both switching transistors are turned on. The both diodes inserted in the collector leads keep back inverse currents.

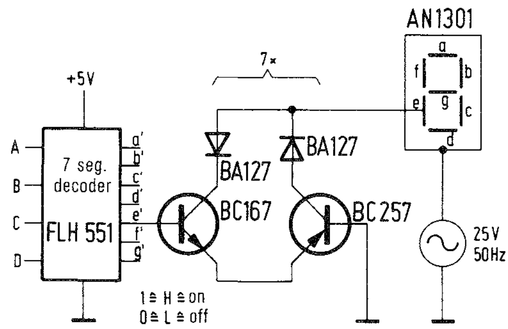


Fig. 4.9.2

4.10 Switches with thyristors

Although under normal conditions thyristors are conductive during the positive half-wave of the current, a conducting anode-gate-path during the negative half-wave can be achieved for special types by impressing a sufficiently high gate-cathode current. Therefore the anode-gate-path can serve as a switch, as shown in **fig. 4.10.1**.

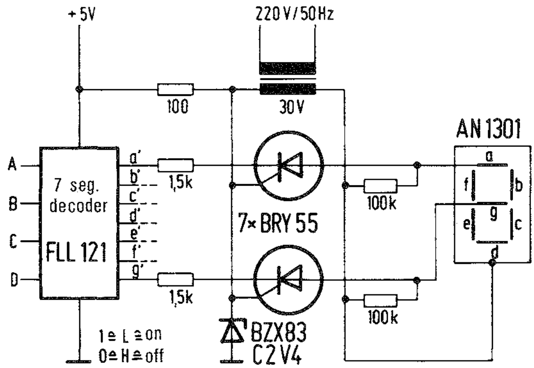


Fig. 4.10.1

The voltage drop at the miniature thyristor BRY 55 is kept below 100 mV at segment currents up to about 1 mA. These currents are sufficient to drive also larger displays.

The TTL-detector has an open collector-output, which shows during the active state a L-level. Gate-cathode currents of about 1 mA are forced to flow through the 1.5-kΩ-resistors. The gate-terminals are connected to a fixed level of about 2.5 V. During the non-active state the cathode current of the thyristor is not permitted to flow.

4.11 LCD for TV-receivers

As an example for supplying an ac voltage to the segments, an indication circuit for 8 TV channels of a receiver is shown in **fig. 4.11.1**. It operates in combination with the touch-IC SAS 560 or SAS 580. A single bipolar transistor serves as a switch.

This is achieved due to the fact that the ac voltage which is to be switched is unsymmetrically clamped to zero level. The symmetrical shape of the square-wave voltage is obtained by the 0.1-μF-capacitors.

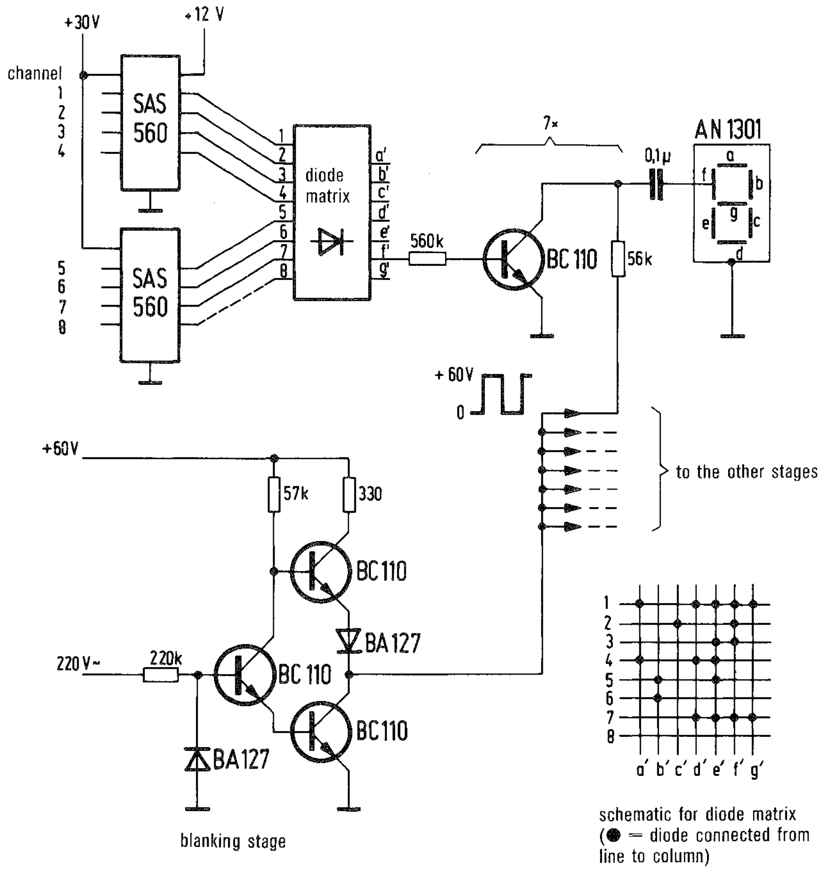


Fig. 4.11.1

The supply voltage of the blanking stage is +60 V, since this is an operating voltage usually prefered. The blanking frequency of 50 Hz is taken directly from the mains.

The decoding of the information for the 7-segment display is attained by a diode-matrix. The touch-IC supplies a positive voltage of 30 V when a channel is chosen. Via the diodes a base current is supplied to those switching transistors, the corresponding segments of which are not to be energized. The turned-off transistors shorten the 50-Hz-voltage. For channel 8 no connection between touch-IC and diode matrix is required, since in this case no segment has to be blanked.

The circuit can be extended to twelve or more channels without any difficulties.

4.12 MOS-circuits for liquid cristal displays

Today integrated circuits in P-MOS or C-MOS technology are mostly used for the operation of LCDs. As against TTL-technology the MOS-technology offers the advantage that bidirectional switches can easier be realized. Besides that a higher output ac-voltage is available. C-MOS-ICs have the lowest power consumption, but they are only suitable for voltages up to max. 15 V. P-MOS-ICs are able to supply output voltages of about 25 V_{pp}. Their power consumption, however, is a little bit higher (between about 10 and 300 mW, according to complexity and manufacturing process).

Circuit with the 10-channel driver-IC, type GDL 121.

This MOS-IC consists of ten similar channels, which include a memory, an exclusive-OR-gate and an amplifier each (cf. **fig. 4.12.1**). All of the inputs are TTL-compatible. The output stages employ push-pull circuits. A supplied square-wave voltage (e.g. f = 50 Hz) is available at the output either in phase or in opposite phase, according to the fact, whether a H-level or a L-level is applied to the input. The output amplitude can amount up to 25 V_{pp}.

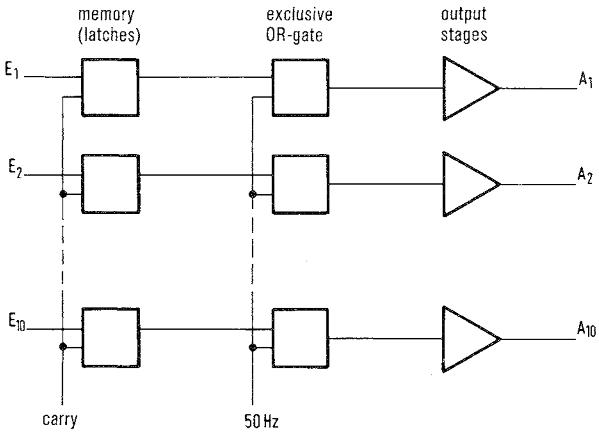


Fig. 4.12.1

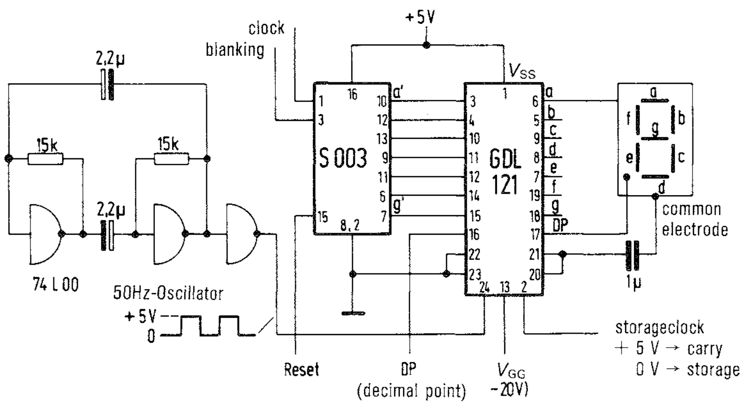


Fig. 4.12.2

A power saving counter is shown in **fig. 4.12.2** as an application sample. In this case the P-MOS-IC, type GDL 121, is combined with a C-MOS counter-decoder-IC, type S 003 (equivalent to CD 4026 A). Eight of the 10 GDL-121-channels are engaged for the control of the segments and the decimal point. Therefore two channels are available for the supply of the common electrode. Thus the relatively high output impedance of about 20 kΩ per channel is halved. The 50-Hz-oscillator operates with the low power TTL-IC, type 74L00, which consumes only a few milliwatts. The power consumption of total circuit is less than 50 mW.

For the display of more decades than one, the inputs of several GDL 121 can be connected in parallel. **Fig. 4.12.3** shows the circuit for a 4-digit-display with 7-segment LCDs. The decoding of the BCD-input is achieved by only one TTL-IC (type FLH 551). The information is supplied sequentially and synchroneously with the memory address to the individual GDL 121-IC.

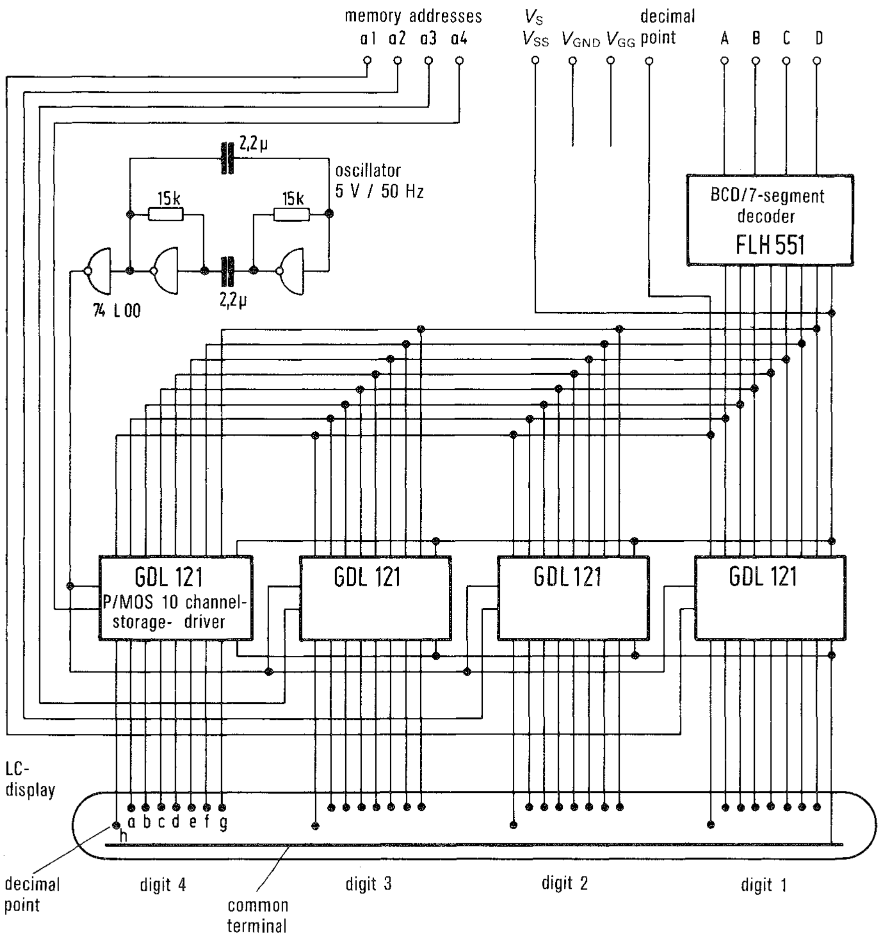


Fig. 4.12.3

Circuit with the counter-memory-decoder-IC, type GDL 101.

In **fig. 4.12.4** a MOS-IC, type GDL 101, is shown. It comprises so-called open-drain-outputs and can be considered as a control circuit according to the sample shown in **fig. 4.8.4**. The connection between terminal 24 (common) and the several segments a to g can either be low-resistive or extremely high-ohmic, i.e. practically interrupted.

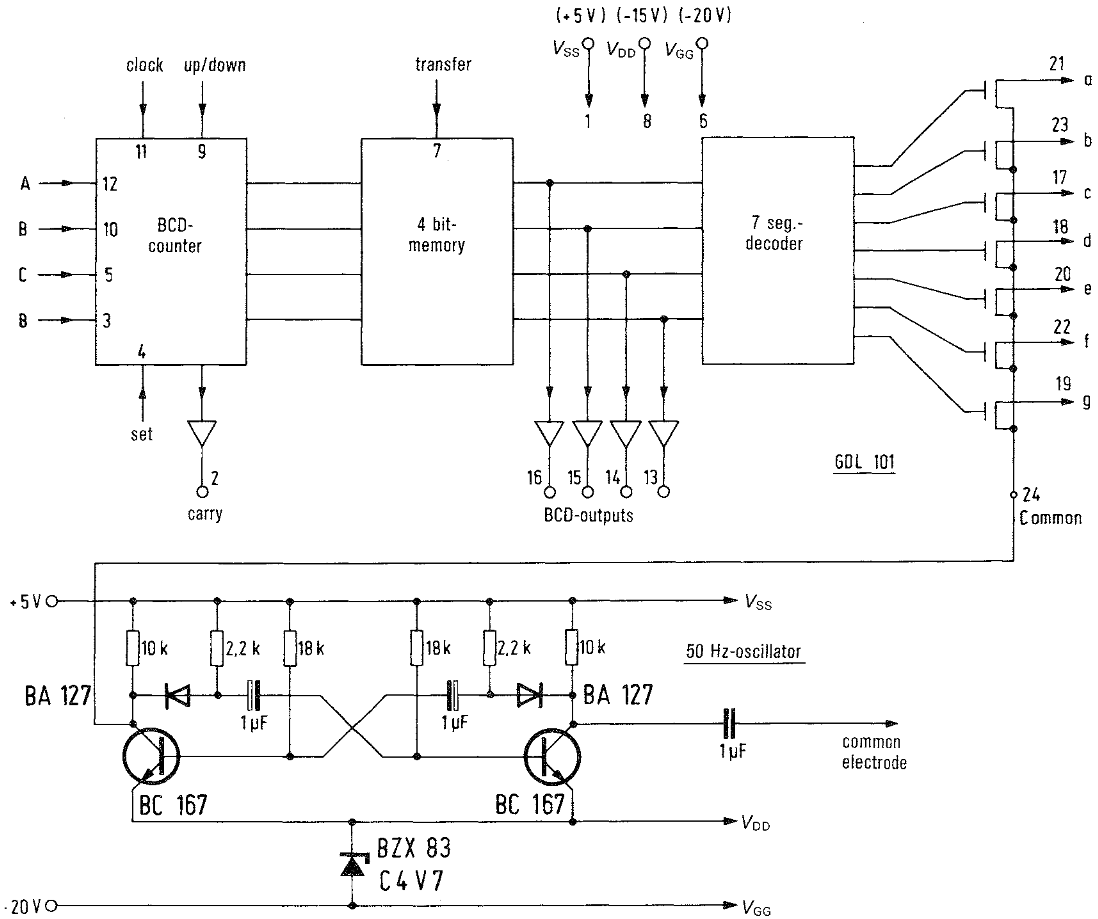


Fig. 4.12.4

The GDL 121 comprises a complete up-down counter with set inputs, memory and a 7-segment decoder. Four BCD-outputs with TTL-level are additionally available. All inputs are also TTL-compatible.

The gate (terminal 6) should have a level which is at least 4 Volt more negative than the one at the drain (terminal 8). If the source of the ac voltage for the common terminal and the common electrode is connected between the terminals V_{DD} and V_{SS}–as shown in **fig. 4.12.4**–then it is achieved that the segment-switches are constantly conductive during the "on"-state. Therefore the common terminal must be more positive by the amount of the source voltage than the gate-voltage.

A capacitor is inserted in the common lead to avoid that unsymmetrical pulses of the 50-Hz-oscillator generate dc contents undesired for LCDs.

Counter with MOS-IC, type 1907.

The feature of the counter-IC, type 1907, allows to drive directly a $3^1/_2$- or 4-digit LCD-device. The 50-Hz-oscillator for the ac voltage is already included. **Fig. 4.12.5** shows a circuit for counting of pulses within a preset time interval (stop watch). The max. pulse frequency is about 300 kHz and a power between 10 and 20 mW is consumed. A gate circuit consisting of C-MOS-NAND-gates enables the inputs of the IC 1907 for the pulses during the gate time. Through the stop-instruction, indicating the end of the gate time, the result of the counting is transfered to the display.

Technical characteristics

Digital-counter-IC
Power-saving counting circuit for AN 5182
(also suited for 4-digit-displays, e.g. AN 4131)

Operating data: $(V_{SS} - V_{DD}) = 8$ to 15 V
$(V_{DD} - V_{GG}) = 8$ to 15 V

Operating voltages for the C-MOS-gate of 4011 AE and 4001 AE are applied from $(V_{SS} - V_{DD})$-supply.

Total power consumption in the static state at $(V_{SS} - V_{DD}) = 8$ V: about 10 to 20 mW.

Max. counting frequency: 300 kHz.

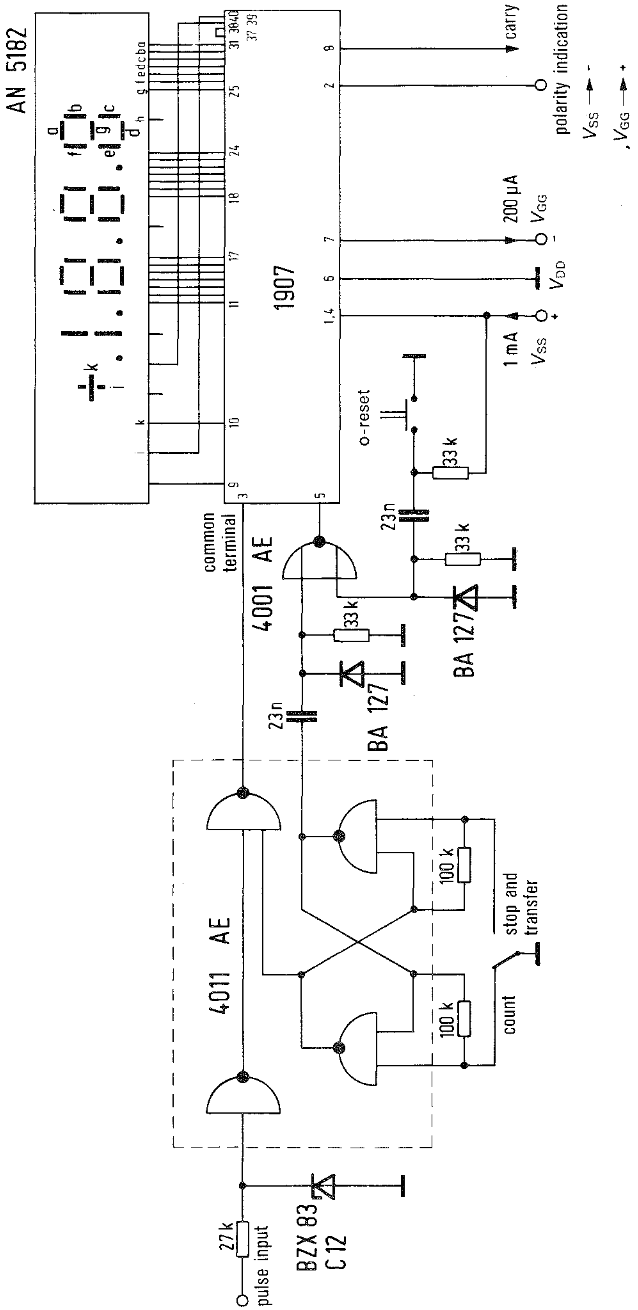

AN 5182
1907
4001 AE
4011 AE
carry
polarity indication
V_{SS} → -
, V_{GG} → +
200 µA
V_{GG} -
V_{DD}
1 mA
V_{SS} +
o-reset
33 k
23n
BA 127
common terminal
100 k
stop and transfer
count
27 k
pulse input
BZX 83
C 12

Fig. 4.12.5

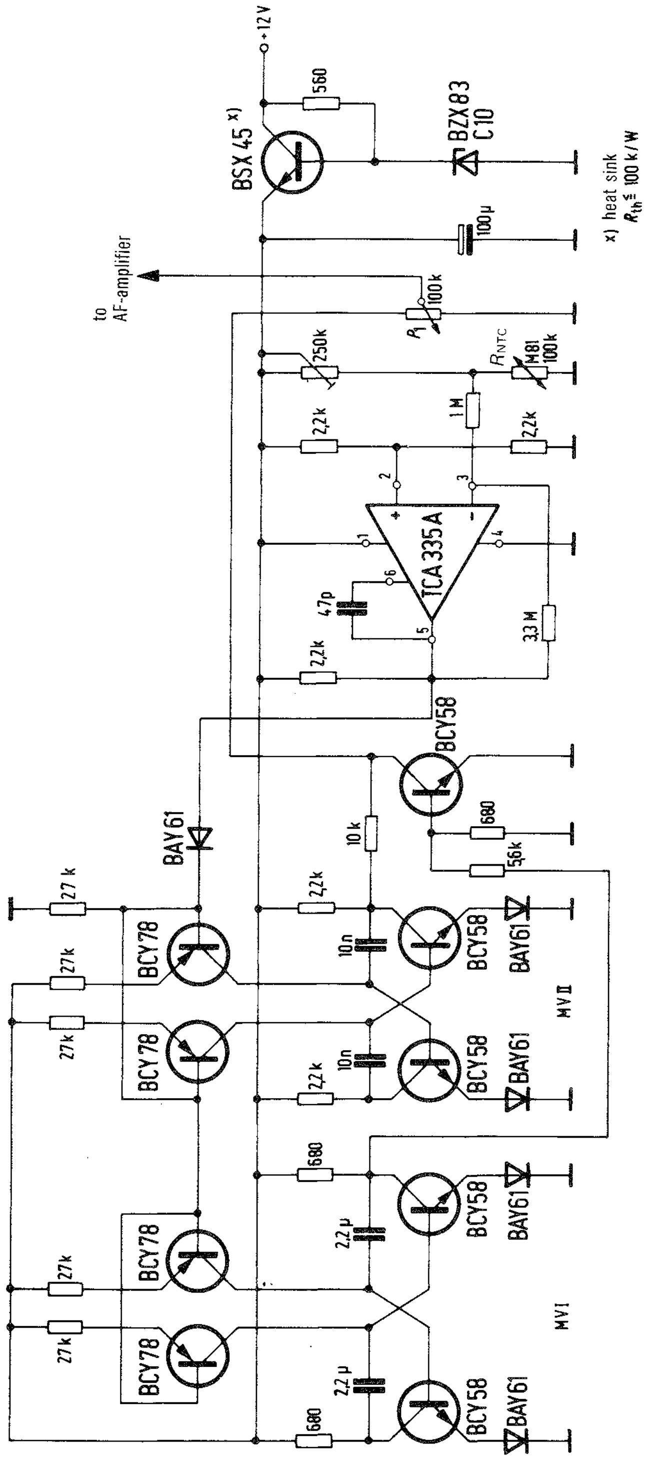

+12 V
560
BSX 45 x)
BZX83
C10
x) heat sink
$R_{th} \leq 100$ k/W
100µ
to
AF-amplifier
100k
R_1
250k
R_{NTC}
M81
100k
1M
2,2k
2,2k
2
3
+
−
1
4
TCA 335 A
6
47p
5
3,3M
2,2k
BCY58
BAY61
10k
680
56k
27k
27k
27k
BCY78
BCY78
2,2k
10n
10n
2,2k
BCY58
BAY61
BCY58
BAY61
MV II
680
BCY78
BCY78
27k
27k
2,2µ
2,2µ
680
BCY58
BAY61
BCY58
BAY61
MV I

Fig. 5.1

5. Control, regulation and switching-amplifier circuits

5.1 Acoustic indicator of temperature changes

Resistance changes of a NTC-resistor can be converted to a frequency variation through the circuit shown in **fig. 5.1**. An oscillation of about 1 kHz is blanked by a multivibrator with a low frequency (5 Hz). Both frequencies change in dependence on the temperature. This signal is amplified in an output amplifier and supplied to a loudspeaker, where it is converted to an audible signal. The temperature is not measured absolutely, only the differences are processed. In principle this circuit is also applicable for conversion of other state changes to an audible signal, if suitable sensors are used, i.e. brightness variations through an optoelectronic detector (photoresistor, photodiode).

In the described application of a temperature indicator the NTC-resistor operates without any load. Thus its resistance depends only on the ambient temperature.

The processing of the temperature-dependent signal is achieved as described in the following. The NTC-resistor is part of a voltage divider, which forms one arm of a bridge at the input of an opamp. The other arm consists of a voltage divider with fixed ratio. The zero adjustment is obtained through the 250-kΩ-potentiometer being in series to the NTC-resistor (about 5 V at the output of the opamp).

The output voltage of the opamp is supplied to both multivibrators via a diode. The base current, impressed by the output voltage of the opamp via the 27-kΩ-emitter-resistors, and the capacitors of 2.2 μF and 10 nF determine the frequency of the multivibrators.

The output voltage of the MV II (about 1 kHz) is blanked by a transistor, which is controlled through MV I (about 5 Hz). This signal is supplied to the input of the output-amplifier via the volume-control potentiometer P_1 = 100 kΩ.

The supply voltage is regulated through a transistor and a z-diode (about 9.5 to 10 V).

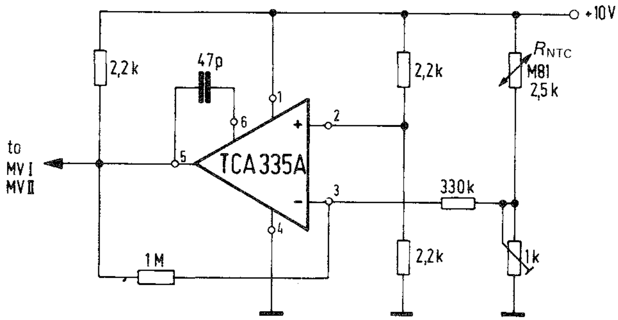
Technical characteristics

Supply voltage V_S	11 to 16 V
Basic frequency MV I f_1	1 kHz
$\Delta f_1 \triangleq (\Delta T \sim \pm 5$ to 6 K)	about $\pm$0.8 kHz
Basic frequency MV II f_2	4 Hz
$\Delta f_2 \triangleq (\Delta T \sim \pm 5$ to 6 K)	about $\pm$3.2 Hz
Ambient temperature T_{amb}	0 °C to 40 °C

5.2 Indicator for flow changes

In contrary to the temperature-change indication described in chapter 5.1, the NTC-resistor is electrically loaded when it is used to detect any flow. The NTC-resistor is differently cooled by different flow velocities of any medium and thus its resistance is changed (cf. **fig. 5.2**).

The following part of the circuit is equal to the one for the indicator of temperature changes.



5.3 Inductive proximity switch with controlled oscillator

Fig. 5.3 shows the circuit of a dynamic, inductive proximity switch.

It consists of an amplitude-controlled oscillator, which is applicable in a wide range of supply voltages and of temperatures. The TCA 105 operates as rectifier and as threshold switch.

Inductive proximity switches which are to react at distances more than 10 mm are difficult to realize, because:

a) an increasing distance requires a rising pot core diameter. The relation is non-linear, therefore the proximity switches have to be operated at their maximum distance to limit the pot core

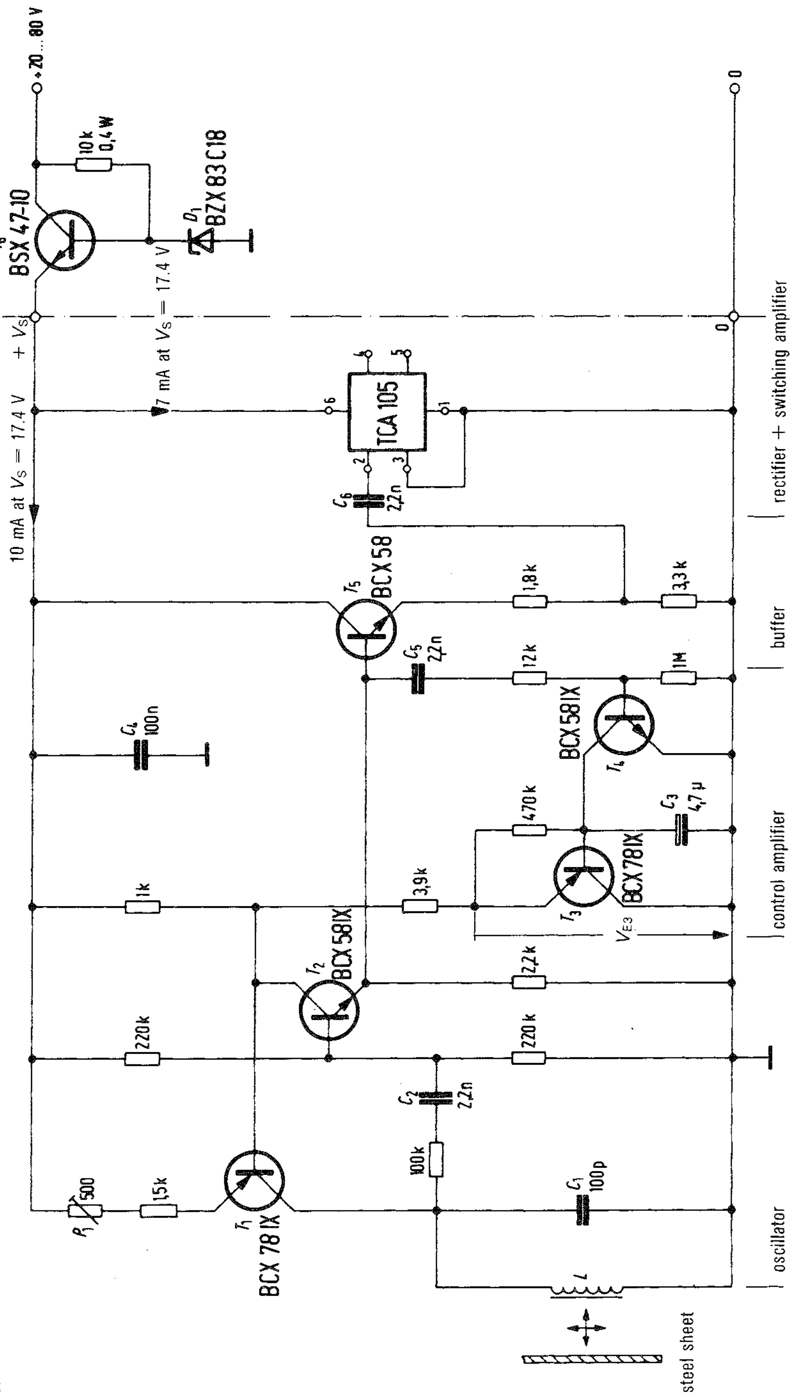

+20 ... 80 V
0
10k 0,4 W
T_6 BSX 47-10
D_1 BZX 83 C18
+ V_S
10 mA at V_S = 17.4 V
7 mA at V_S = 17.4 V
V_S = 17.4 V
TCA 105
C_6 2,2n
T_5 BCX 58
1,8k
3,3k
C_5 2,2n
12k
1M
C_4 100n
T_4 BCX 58IX
470k
C_3 4,7 µ
1k
3,9k
T_3 BCX 78IX
V_{E3}
T_2 BCX 58IX
2,2k
220k
220k
C_2 2,2n
100k
R_1 500
1,5k
T_1 BCX 78IX
C_1 100p
L
steel sheet
rectifier + switching amplifier
buffer
control amplifier
oscillator

Fig. 5.3

to a reasonable seize. **Fig. 5.3.1** shows the distance $a_{0.71}$ of an iron sheet in dependence on the outer diameter of a pot core. $A_{0.71}$ is defined as the distance at which the Q of the coil has reached a value of 71% of Q_0, which is the quality factor without any attenuation ($Q = 0.71 \times Q_0$).

b) component tolerances, supply voltage fluctuations and temperature changes can cause an interruption of the oscillation, if the proximity switch runs at its sensitivity limit.

A control circuit for stabilisation of the oscillator amplitude enables the construction of proximity switches which operate up to their sensitivity limit.

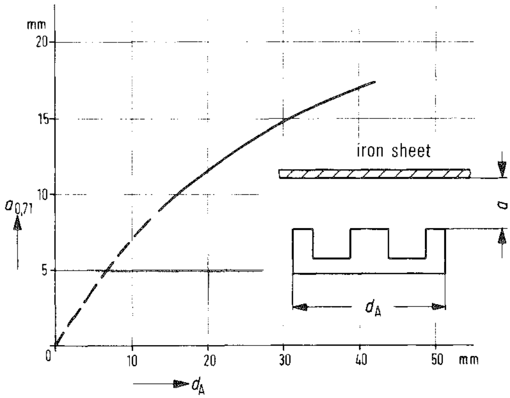


Fig. 5.3.1

Distance $a_{0.71}$ of an iron sheet in dependence on the outside diameter of a pot core,
$a_{0.71}$ = distance at which the coil quality factor is $Q = 0.71 \times Q_0$.
Q_0 = quality factor of the non-damped coil

The oscillator consists of the L-C-resonant-circuit and the transistors T_1, T_2. As inductor serves an open pot core half, 36⌀ × 22. The coil quality factor is reduced by the approached iron sheet. The coil is wound on one half of a double-section bobbin. The gain of the oscillator and the operating point of the control circuit are adjusted by the potentiometer P_1.

The amplitude control is achieved through the transistors T_3 and T_4. If the output-amplitude increases, the transistor T_4 is turned on via C_5. Transistor T_3 lifts the base level of T_1 and thus the amplitude is reduced. The capacitor integrates the rf-pulses and determines the oscillator control time, which is about 1 s. Due to this long time the proximity switch still reacts even if the objects pass relatively slow.

Transistor T_5 operates as an impedance transformer and separates oscillator and rectifier.

As rectifier and threshold switch the IC TCA 105 has been chosen. Its antiphase outputs (pin 4 and 5) can be loaded with 50 mA each.

If only an extended supply voltage range of V_S = 20 to 80 V is available, the operating voltage has to be regulated by a transistor T_5 and a diode D_1.

All capacitors are ceramic ones with the exception of C_3. This is an electrolytic capacitor.

Alignment procedure

V_B = 17.5 V : adjust the voltage $V_{E\,3}$ = 5 V at the control amplifier through potentiometer P_1.

Technical data:

Operating voltage	
(without voltage control, T_{amb} = 25 °C)	17.5 V (12.5 to 21 V)
Supply current	≈17 mA (12.5 to 20.5 mA)
Temperature range (V_B = 15 to 19 V)	−25 to +60 °C
Max. switch distance	18 mm
Frequency of oscillation	1 MHz
Time constant of the oscillator	
oscillation turn-on	≈0.4 ms
Oscillation turn-off	≈1 ms
Control time of oscillator	≈1 s

5.4 Circuits achieving delay times between 0.2 and 100 s

Operational amplifiers with a Darlington input are favoured particularly for delay networks. The following circuit, designed for a special application, achieves delay times between 0.2 and 100 s **(fig. 5.4)**. The recovery time of less than 250 ms is relatively short. The delay process starts when the supply voltage (+12 V) is applied to the circuit.

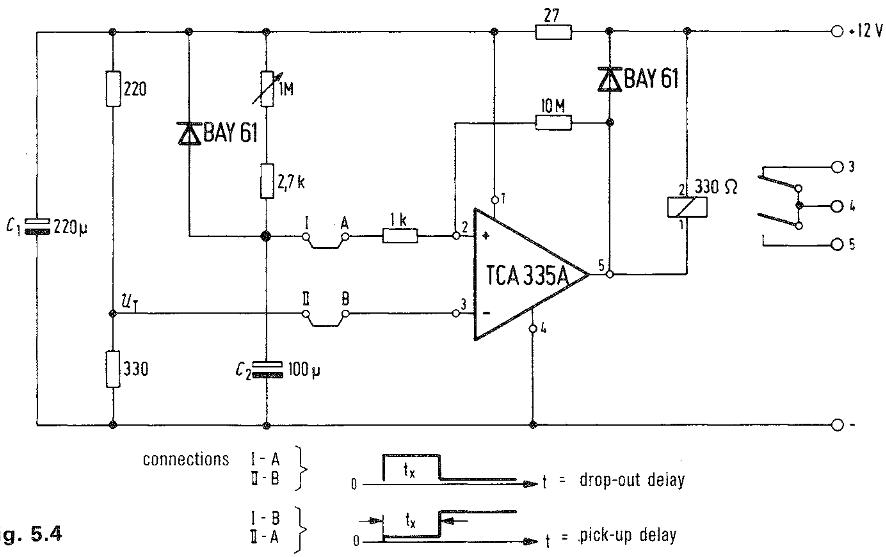


Fig. 5.4

Without any additional transistor-amplifiers the opamp-IC, type TCA 335 A, is able to drive directly a card-relay, acting as a load in this case. If the terminals I and A as well as II and B are connected a drop-out delay is obtained. If, however, the connections are made between I and B, II and A a pick-up delay will be achieved.

Technical data:

Supply voltage	10 to 16 V
Supply current	55 mA
Delay time, adjustable	0.2 to 100 s
Return time	< 250 ms
Output power	~2 kVA
	= 50 W

Operating ambient temperature	0 to 70 °C
Storage temperature	−40 to +125 °C
Relay	E V23027-A0002-A101
Capacitor C_1, 220 μF	B41283-A4227T
Capacitor C_2, 100 μF	B41588-B4107T

5.5 Voltage-to-frequency converter

The described voltage-to-frequency converter **(fig. 5.5)** consists of an integrator, a comparator and a switch. A saw-tooth voltage which is proportional to the input voltage is available at the output of the integrator. The comparator output supplies a needle pulse with a duration of about 5 μs and with an amplitude corresponding to the operating voltages. An additional amplifier may be connected infront of the integrator. Thus the converter input becomes high-ohmic and independent of any generator source. It is achieved by suitable dimensioning of the circuit that the frequency deviation varies with the output level.

Assuming that the capacitor C_0 is charged at the moment in accordance with the polarity indicated in the figure, it is discharged with a constant current $I_C = \frac{V'_{in}}{R_0} - I_{in}$. The integration time t_i for the output voltage of the integrator is as follows:

$$I_C \times t_i = V_{CO} \times C_0$$

with $I_C = \frac{V'_{in}}{R_0} - I_{in}$ and $V_{CO} = -V_{B-} - V_{CE\ rest\ T1}$

$$t_i = \frac{(-V_{B-} - V_{CE\ rest\ T1}) \times C_0 \times R_0}{V'_{in} - I_{in} \times R_0}.$$

If C_0 is discharged to a certain level at which the potential of the inverting input is lower than the zero level at input 2, then the output is switched off and the inverting input is connected to V_{B-} through the transistor T_1. The capacitor C_0 is now charged with a time constant of $\tau_c = C_0 \times R_L$. If its voltage reaches the value $V_{CO} = -V_{B-} - V_{CE\ rest}$, the comparator is turned on again and switches off the transistor. Now the discharging of C_0 begins.

For the return time t_r applies:

$$t_r = R_L \times C_0 \times \log_e \frac{V_{B+} - V_{B-} - V_{CE\ rest}}{V_{B+}}$$

This return time, however, is superimposed by a delay time t_v, which is determined by C_f and C_{Tr} (for frequency compensation), by the current gain of the integrator Darlington-output and that of the switching transistor as well as by the integrator-IC itself. Therefore the voltage at the integrator output does not jump to V_{CO} immediately, when the switching transistor is turned off. The same happens to the level of the integratorinput 3 falling accordingly to zero potential. A capacitance decrease of C_f reduces this time delay.

If no preamplifier is used, the resistor R_0 is replaced by a 25-kΩ-potentiometer, through which the output frequency of the converter is adjusted to a value of 500 Hz at an input voltage V_{in} = 500 mV. The resistance of R_0 includes also the generator impedance of V_E, whereby the offset adjustment is achieved at terminal 2 of the integrator.

If a preamplifier is used, the converter is adjusted through the potentiometer P, whereby the voltage gain of the preamplifier is varied accordingly. The offset compensation is now achieved commonly for the preamplifier and the integrator at input 3 of the preamplifier, whereat the resistance of R is reduced to 680 kΩ (dashed line).

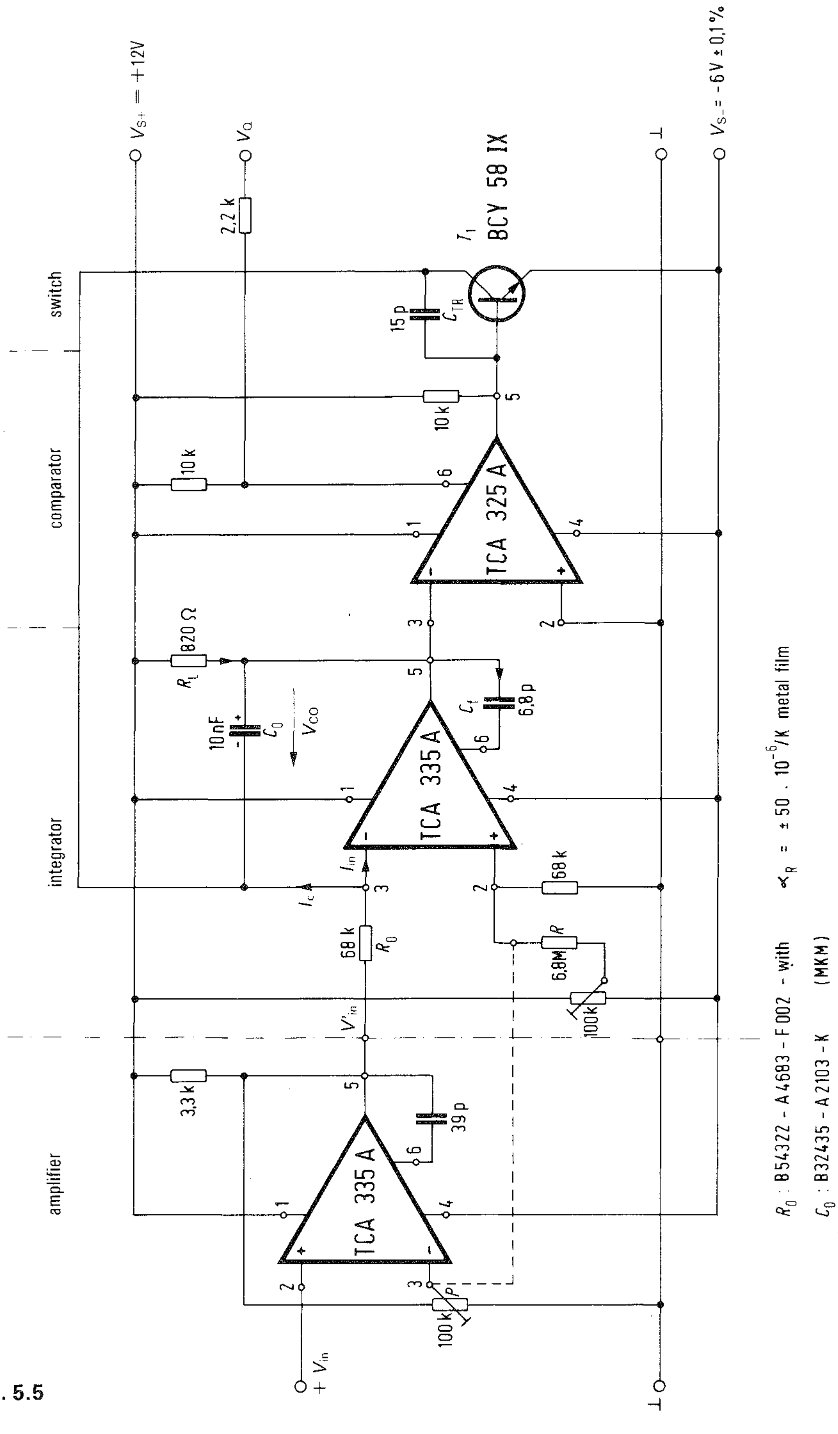

amplifier
integrator
comparator
switch
$V_{S+} = +12V$
V_Q
$V_{S-} = -6V \pm 0,1\%$
T_1
BCY 58 IX
15 p
C_{TR}
2,2 k
10 k
10 k
TCA 325 A
TCA 335 A
TCA 335 A
820 Ω
R_L
10 nF
C_0
V_{CO}
C_1
6,8 p
I_{in}
I_c
68 k
R_0
68 k
R
6,8M
100 k
V'_{in}
3,3 k
39 p
P
100 k
$+ V_{in}$
R_0 : B54322 - A4683 - F002 - with $\alpha_R = \pm 50 . 10^{-6}$/K metal film
C_0 : B32435 - A2103 - K (MKM)

Fig. 5.5

A change of the frequency deviation is obtained by adequate variation of C_0 and R_0 or P. For smaller frequency deviations, e.g. 0 to 100 Hz, the product $C_0 \times R_0$ has to be increased by a factor of 10. If C_0 is increased, the error rises at higher frequencies (longer return time). If R_0 is raised, the error becomes greater at lower frequencies.

The tolerance of V_{B-} influences the error of the integration time directly. The integrator input current I_{in} can be neglected at higher values of the measuring voltage V'_{in}; at lower levels of V'_{in}, however, the error is caused mainly by I_{in}. At high input voltages, errors are generated by the return time. A resistance decrease of R_L reduces the charging time t_r of the capacitor C_0 and the delay time t_v. A limit, however, is given by the power dissipation of the TCA 335 A. If the capacitor C_f for the frequency compensation could be omitted, the delay time t_v will be zero.

Fig. 5.5.1 shows the linearity error of the circuit, proportioned with the preamplifier.

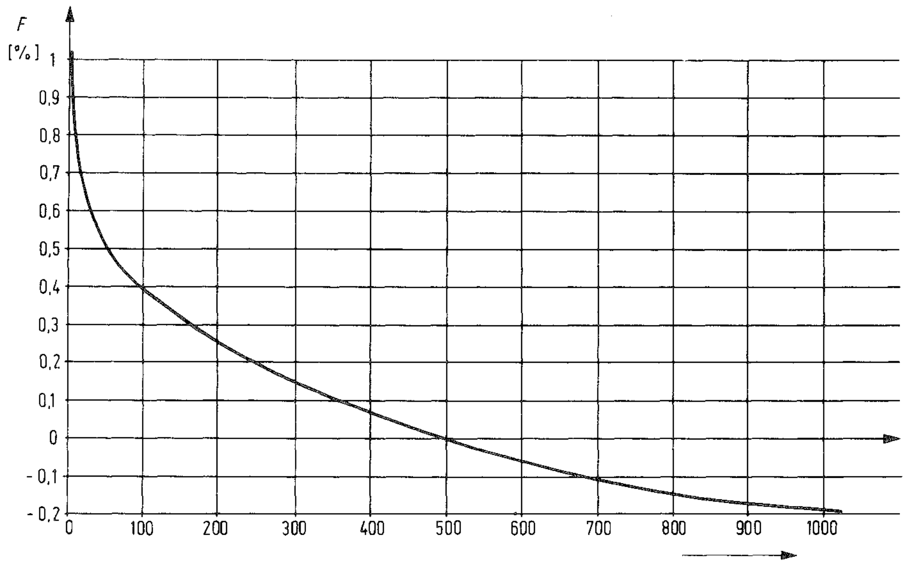
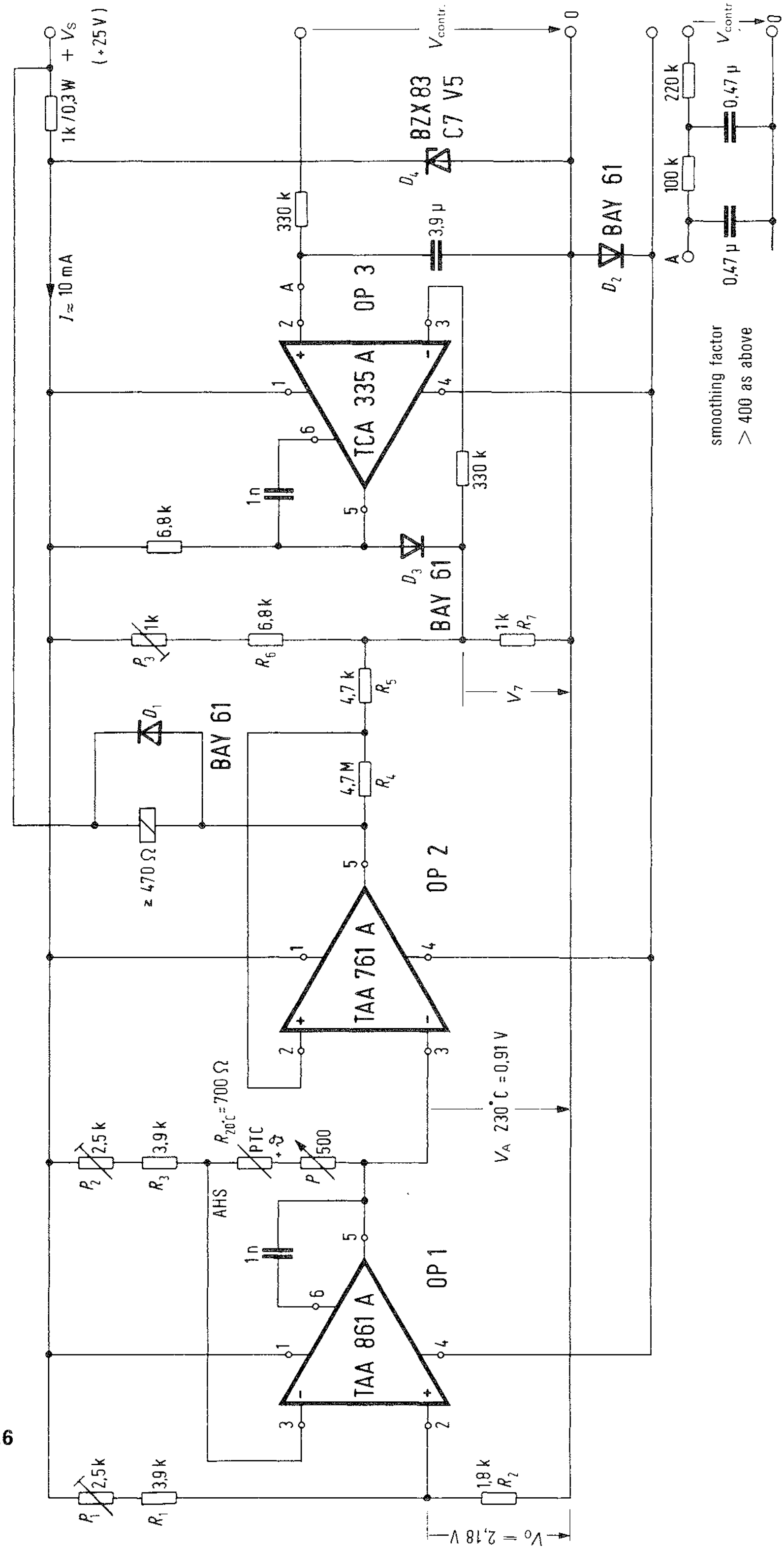


Fig. 5.5.1

Technical data:

Supply voltages	V_{B-}	−6 V ±0.1%
	V_{B+}	+12 V ±1%
Supply current at V_{B-}	I_{B-}	2 mA
V_{B+}	I_{B+}	21 mA
Temperature range	T_{amb}	−25 °C to +70 °C
Input voltage	V_{in}	0 to 1 V
Output frequency	f	0 to 1000 Hz
Needle pulses		
Duration: 5 μs		
Amplitude: $V_{B+} - V_{B-}$		
Accuracy (V_{in}> 10 mV)		<1%
R_0: B54322-A4683-F002		
α_R = ±50×10^{-6}/K metal film		
C_0: B32435-A2103-K (MKM)		



$+V_S$ (+25 V)
1k/0,3 W
$I \approx 10$ mA
$V_{contr.}$
0
BZX 83 C7 V5
D_4
330 k
3,9 µ
BAY 61
D_2
A
220 k
100 k
0,47 µ
smoothing factor
> 400 as above
OP 3
TCA 335 A
1n
330 k
6,8 k
D_3
BAY 61
P_3 1k
R_6 6,8 k
1k R_7
V_7
4,7 k R_5
D_1
BAY 61
4,7 M R_4
≈ 470 Ω
OP 2
TAA 761 A
V_A 230 °C = 0,91 V
$R_{20°C}$ = 700 Ω
PTC
500
P_2 2,5 k
R_3 3,9 k
AHS
OP 1
TAA 861 A
P_1 2,5 k
R_1 3,9 k
1,8 k R_2
V_0 = 2,18 V

Fig. 5.6

5.6 Control circuit for storage space heaters

In the design examples, known today, an afterheat sensor (AHS) is used as a voltage divider. But with this configuration a linear characteristic can not be attained. With the circuit, shown in **fig. 5.6**, afterheat devices with a linear characteristic can be realized. Several units can be driven selectively by one external control device. It supplies a dc voltage which depends on the environmental conditions and which ranges between 0.91 and 1.43 V. The switching voltage V_7 at the input 2 of the OP 2 is 0.91 V. It is determined by the divider ratio $(P_3+R_6)/R_7$ at $V_{\text{Contr.}} = 0$ V. Control voltages >0.91 V are applied to the voltage V_7 by the OP 3.

On account of the high resistance of the 330-kΩ-resistor connected in series to the control voltage source, the "Darlington" operational amplifier TCA 335 A is used. Its input current is only 20 nA. The output-voltage error, created by the input offset-current, is in the range of about ±3 mV. The input offset-voltage results in an additional error of ±10 mV. The required, negative supply voltage of 0.6 V is produced by the diode D_2. If the ac voltage superposed to the control voltage should be too high, a double-filter circuit will be advantageous.

A constant current is impressed to the afterheat sensor through the OP 1. There by a linear characteristic of the output voltage V_A, depending on the resistance of the PTC-resistor, is achieved.

If the voltage V_0 is adjusted correctly, the output voltage V_A, generated by the AHS, corresponds to the control voltage deviation, so that no additional division of the control voltage is required.

The voltage V_0 is calculated through the following equation:

$$V_0 = \frac{1-(a \times b)}{a-(a \times b)} \times V_{A\,(230\,°C)}\,.$$

$$\text{With } a = \frac{V_{\text{contr. min.}}}{V_{\text{contr. max.}}} = \frac{0.91}{1.43} = 0.637\,,$$

$$b = \frac{R_{AH\,(20\,°C)}}{R_{AH\,(230\,°C)}} = \frac{700\,\Omega}{1200\,\Omega} = 0.584$$

and $V_{A\,(230\,°C)} = V_{\text{contr. min.}} = 0.91$ V follows $V_0 = 2.18$ V

Fig. 5.6.1 shows the characteristic of the circuit. If $V_{\text{contr.}}$ is equal or less than 0.91 V, the hysteresis will be increased by about 20%, since the resistance of R_7 becomes effective in this range. If this influence is not desired, either the resistances of R_4 and R_5 have to be increased or the divider consisting of P_3, R_6, R_7, has to be proportioned with lower resistances.

Adjustment procedure

a) adjust $V_0 = 2.18$ V through P_1

b) adjust $V_{A\,(230\,°C)} = 0.91$ V through P_2 at $R_{AH\,(230\,°C)}$ and $P = 0\,\Omega$

c) adjust $V_7 = 0.91$ through P_3 at $V_{\text{contr.}} = 0$ V.

The accuracy depends on the stability of the z-voltage. If required, the terminal 1 of each opamp can be connected to an unstabilized supply voltage.

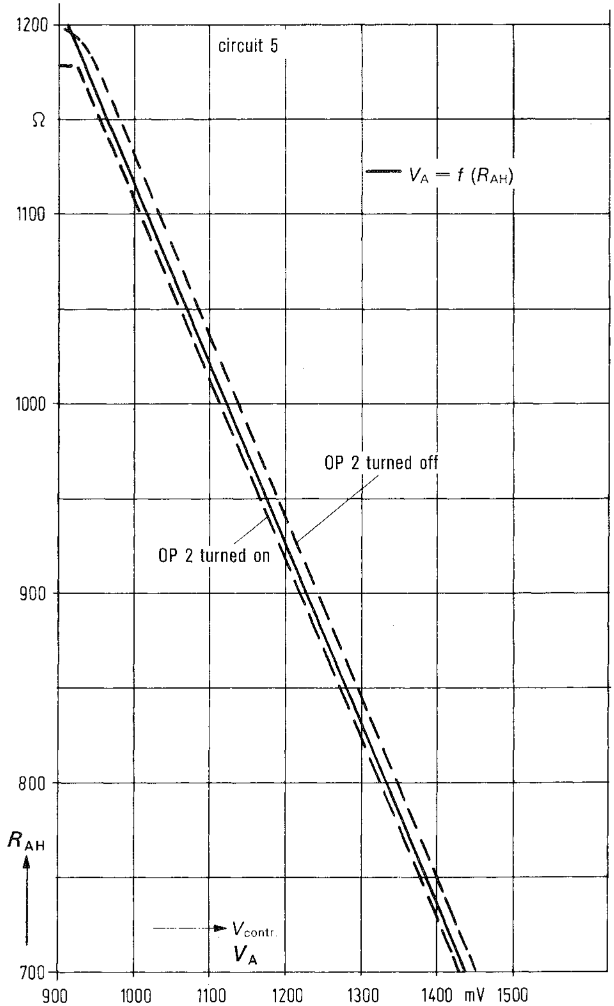


Fig. 5.6.1

5.7 Short-circuit-proof switching amplifier for 24 V/2 A

If solenoid valves are switched with a relatively high frequency, the inductive voltage peaks can not be clipped by means of diodes, since inadmissible drop-out time delays will occur. Two switching amplifiers are described; one of both is short-circuit-proof. In both cases the output stages employ triple-diffused transistors. The inductive voltage peaks are limited only at about 200 V.

Fig. 5.7 shows a circuit of a switching amplifier using the triple-diffused transistor BUY 77. In order to reduce the switching power loss of the transistor a capacitor with small capacitance is connected between its collector and emitter terminal. In addition a parallel z-diode limits inductive voltage peaks, if these should occur at the load and exceed a value of about 200 V. Thus any danger for the transistor is eliminated. The output transistor is driven by the transistor BSV 15–16. Therefore the required control input current is less than 2 mA.

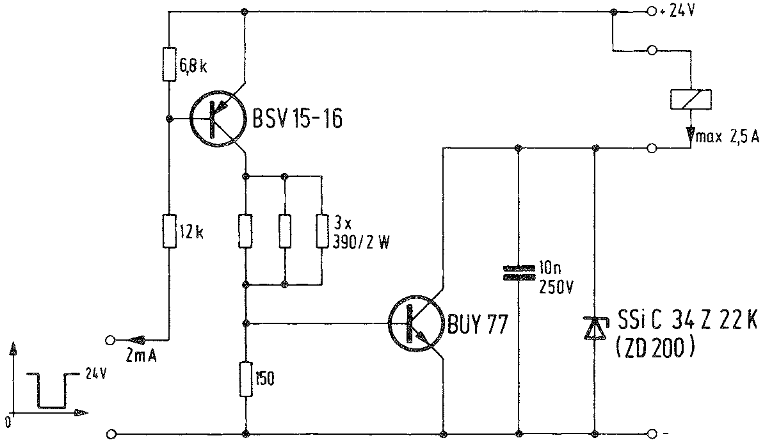


Fig. 5.7

The circuit shown in **fig. 5.7.1** is the same with the exception of the two additional prestage transistors BCY 78 and BCY 58. Through this pre-circuit the amplifier becomes short-circuit-proof.

If the selenoid valve connected to the amplifier output is shorted, the collector voltage of the BUY 78 does not drop to the saturation voltage value (< 1 V), it remains, however, at +24 V when the amplifier is switched on. Thus the transistor BCY 58, connected to the collector of the BUY 77 via the 220-kΩ-resistor and the diode BAY 44, is turned on and switches off the control current of the actual power amplifier transistor BUY 77 via the transistor BSV 15–16. The output transistor remains turned off without any danger. This short-circuit protection is effective also during the switching operation. It reacts to overloads as soon as the voltage at the collector of the output transistor rises to a value of 1 to 1.5 V.

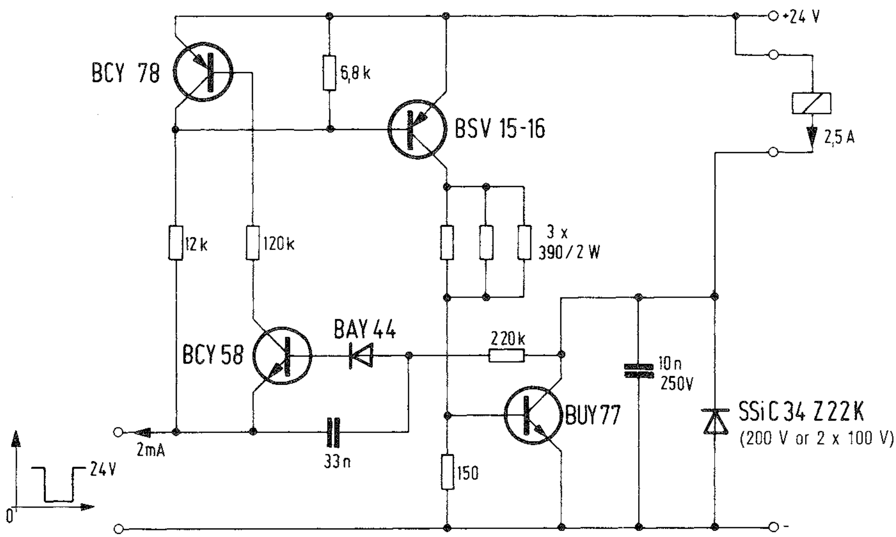


Fig. 5.7.1

Technical data:

V_S	24 V
I_{switch}	2.5 A
$V_{contr.}$	24 V
$I_{contr.}$	2 mA

5.8 Excess temperature protection circuit with mains-operated PTC-resistors

Certain power supply devices have to be protected against influences of too high temperatures. In the dangerous range the mains voltage is to be interrupted, i.e. the supply of energy is to be stopped. **Fig. 5.8** shows a temperature protection circuit, which is a good using a triac and a PTC-resistor.

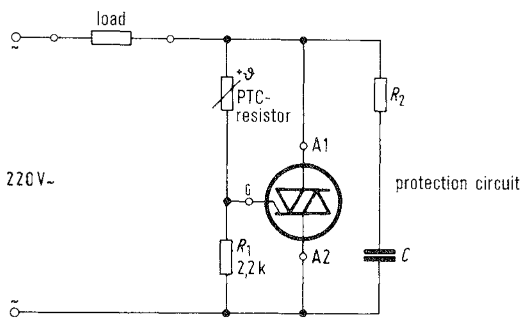


Fig. 5.8

PTC-resistors arc characterized by a relatively low resistance below their initial temperature. Above it, their TC is positive. It increases rapidly above the nominal temperature and the final resistance can amount several Mega-ohms.

For the resistance rise of a PTC-resistor it is of no importance whether the heat is supplied externally or internally. In the latter case this means self-heating.

As demonstrated in the following example the PTC-resistor is connected between anode and gate of a triac. If an ac voltage is supplied to the complete circuit, the triac is triggered immediately after each zero-axis crossing, i.e. it is turned on continuously. Self-heating of the PTC-resistor can not occur, since the low residual voltage V_{A2}–V_{GA} is applied to it.

If, however, the PTC-resistor is warmed over its nominal temperature due to external heat influences, it becomes rapidly more high-resistive. Thus the triggering threshold of the triac is shifted away from the zero-axis crossing of the ac voltage with respect to time. The pulse-shaped, partially cut sine half-waves of the voltage heat the PTC-resistor additionally. Through this temperature feedback the PTC-resistor gets at least such a high-resistance, that the triac discontinues to trigger. Thereby the load is turned off.

If the resistor R_1 has such a low resistance that the total holding current of the PTC-resistor is enabled to flow then the circuit is locked, even if the external temperature influence is eliminated.

Technical data: V_S 220 V~

max. load.	Rated temp.	PTC-resistor	Triac	R_2	C
220 W	60 °C	P 330-B 22 P 330-B 20 P 350-B 21 P 350-B 20	TXC03A60	470 Ω	0.1 μF
	80 °C				
600 W	60 °C	P 330-B 22 P 330-B 20 P 350-B 21 P 350-B 20	TXC02A60	330 Ω	0.22 μF
	80 °C				
1200 W	60 °C	P 330-B 22 P 330-B 20 P 350-B 21 P 350-B 20	TXC01A60	220 Ω	0.33 μF
	80 °C				

5.9 Level indicator for the brake fluid of a car

The fluid in a tank of a braking system is not to fall below a minimum level to assure a faultless operation of the brakes.

The electronic protection circuit **(fig. 5.9)** indicates by means of a warning light and a buzzer when an inadmissible decrease of the brake fluid occurs (probably caused by a fraction of the brake line). Both circuits of a two-circuit brake system are controlled.

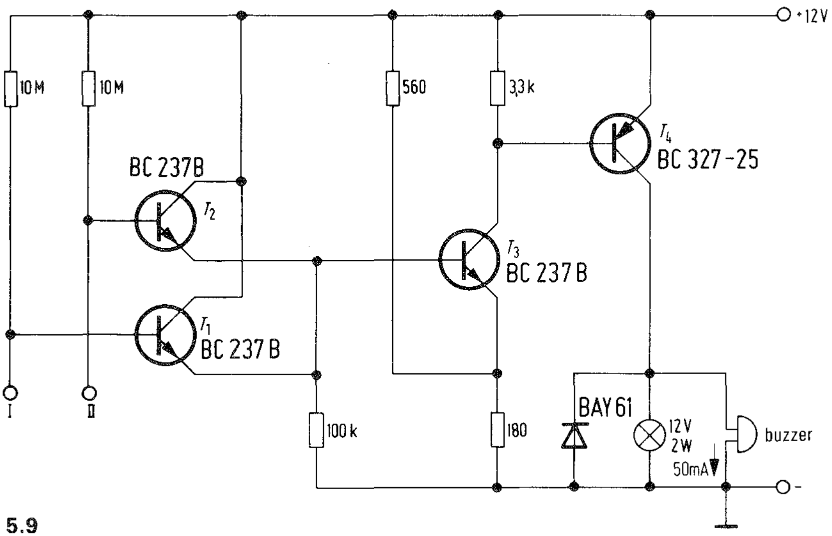


Fig. 5.9

The picture shows the schematic of the protection circuit. In each of the two tanks a metal sensor-electrode (e.g. brass) is installed in the way, that it extends to the minimum level. In case that both electrodes are dipped into the brake fluid no indication occurs. If a brake fluid loss should happen, probably by a leaky cylinder or by a pipe burst, the electrodes are no longer surrounded by the fluid. The lamp or the buzzer are turned on.

If only the electrode I is dipped into the fluid, the control current flows through the liquid to the case of the brake cylinders and then to ground (cf. **fig. 5.9.1**). In case that the fluid level drops as far as the electrode is no longer dipped in, then transistor T_1 becomes conductive and controls via transistor T_3 the output transistor T_4, i.e. lamp and buzzer are turned on. The same operation applies adequately to electrode II.

The control current of the sensors is 1.4 μA. This is a very low value, however, it was chosen due to the fact that the system has to operate even at minus temperatures (−25 °C), when the conductivity of the brake fluid is lower.

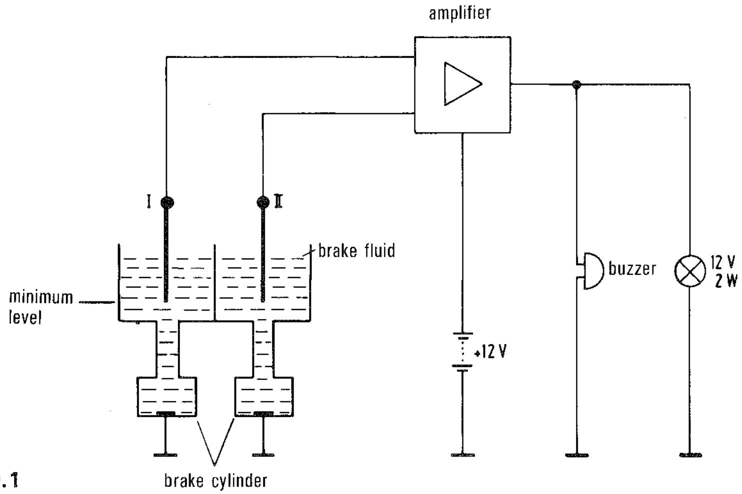


Fig. 5.9.1

Technical data:

V_S	8.5 to 16 V
Lamp current	170 mA
Lamp starting peak current	750 mA
Buzzer current	approx. 50 mA
Permissible ambient temperature	−25 °C to +100 °C

5.10 Transistorized ignition system with electronic speed governor

As far as possible the nominal speed of a petrol engine should not be exceeded. The electronic circuit of the speedometer shapes and integrates the pulses, generated by the interrupter, into a dc signal which is a function of the speed and can be used to turn off the ignition.

The tachometer shown in **fig. 5.10** is designed for a six-cylinder four-stroke cycle engine. The speed is indicated by a voltmeter. The potentiometer R_1 is used for adjustment and 1 Volt corresponds exactly to a speed of 1000 r.p.m.

The basic circuit of the tachometer is a monostable multivibrator. When the supply voltage is applied while the ignition system is not turned on, the transistor T_2 is switched on via resistor R_1. Transistor T_1 is turned on through resistor R_1 and T_3 is turned off. Consequently there is no signal at output A. Whilst the interrupter is open during operation of the ignition system, short positive needle-pulses are applied via capacitor C_2 and diode D_1 to the base of transistor T_1, thereby switching it off at regular intervals. Since the operating voltage is always higher than the tachometer voltage, stabilized by a z-diode, a positive current can flow.

The transistor T_1 remains turned off, however, not only during the needle pulses but also during the total off-time of the monostable multivibrator. The off-time is determined essentially by the time constant of the R_1/C_1-circuit. Capacitor C_1 is charged very rapidly when transistors T_1 and T_2 are switched on. During its discharging a reverse voltage is applied to the base of transistor T_2 via the resistors R_1 and R_4.

Since the transistor operates in opposition to the multivibrator, the off-time acts as pulse time at its collector (output A_1). It has to be pointed out that the pulse time is somewhat shorter (e.g. 90%) than the shortest sequence of interrupter pulses.

Square-wave pulses are available at output A_1. The average value, indicated by the measuring instrument, corresponds directly to the speed of the engine.

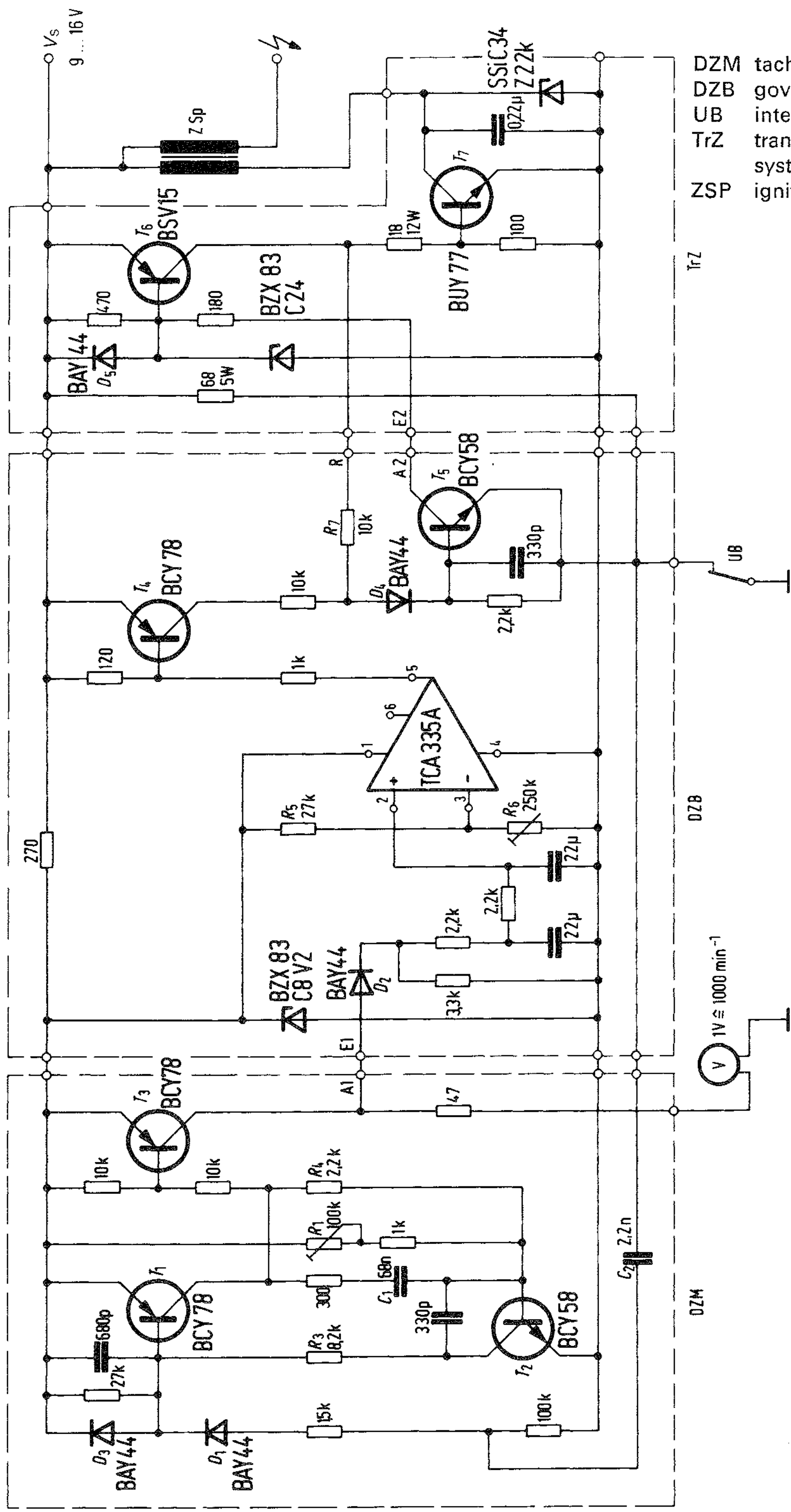
The function of the governor is as follows. At a certain speed the next ignition has to be suppressed and to be turned on again with the smallest possible hysteresis. Moreover no undefined ignitions are allowed to occur at the instant of response. Therefore the governor is essentialy an amplifier with the function of a gate. In the solution shown in **fig. 5.10** the sequence of pulses applied to input E_1 has to be integrated and filtered by the RC-network behind the isolating diode D_2. The resulting dc voltage is reduced somewhat, compared to the value of the tachometer. The opamp TCA 335 A compares the filtered voltage of the tachometer and the voltage of the divider R_5/R_6, whereby R_6 is adjusted so that the opamp TCA 335 A is turned off at the desired maximum speed of the engine.

The amplifier also turns off the transistor T_4 and T_5. Latter blocks input E_2 of the ignition system. Because of the feedback resistor R_7 the transistor T_7 is turned off, only if no current if flowing through the ignition system. Otherwise the next regular ignition takes place before the system is switched off. Thus any undefined ignition is prevented.

In the ignition system the tripple diffused transistor T_7 (BUY 77) drives the ignition coil. During the turn-on state the energy is stored in the ignition coil and transfered to the plugs at the instant of turn-off. The transistor is protected against transients by a 220 V z-diode. Transistor T_6 acts as a driver.

In figs. **5.10.1** a, b, c, d and e the turn-off operation is illustrated. In fig. **5.10.1** a it is shown that the voltage V_n, depending on the speed, has increased to the threshold value of the opamp, which turns off. If the interrupter contacts are open at this moment, the ignition is turned off immediately **(fig. 5.10.1c)**. If the contact is closed during the turn-off, an additional ignition occurs when the contact opens again **(Fig. 5.10.1e)**. The ignition is turned on once more, when the engine speed has dropped to 6500 min^{-1}.

In the following table the technical data of the ignition system are given.



DZM tachometer
DZB governor
UB interrupter
TrZ transistor ignition system
ZSP ignition coil

Fig. 5.10

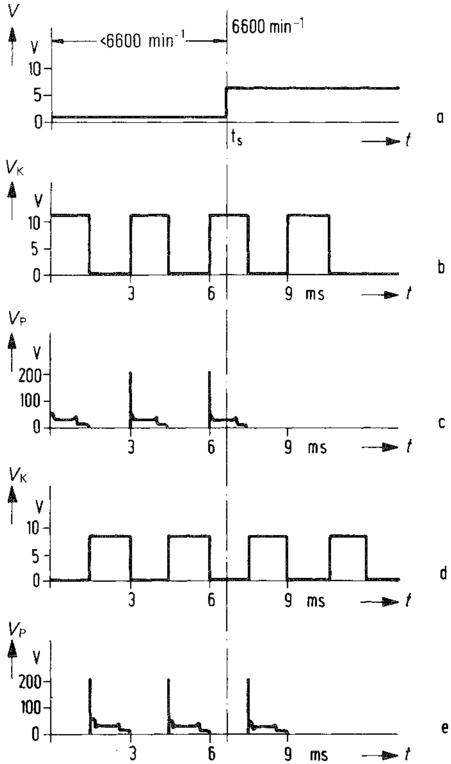


Fig. 5.10.1

Table 5.10.2
Function of the governor

a Threshold 6600 min^{-1}
b Pulses at interrupter contact, which is open at time t_s
c Ignition pulse
d Pulses at interrupter contact, which is closed at time t_s
e Ignition pulses
V_n Voltage at speed n
V_K Voltage at interrupter contact
V_P voltage at primary side of ignition coil

Technical data of the ignition system

Operation voltage	9 to 16 V
Switching threshold	3000 to 6600 min^{-1} adjustable with R_6
Hysteresis	<100 min^{-1}
Internal impedance of tachometer	>1 kΩ
Primary ignition voltage	220 V
Primary ignition current	5 A

5.11 Electronic indicator for battery charging

In modern automobiles, using three-phase generators, the charge indication lamp controls only the function of the generator. An undercharged battery, as it is liable to happen when the automobile has been forced by trafic conditions to proceed by stops and starts, is no longer indicated as former by flickering of the red pilot lamp.

For routine tests of the charging conditions only two threshold values are required. By using two simple amplifiers and two light emitting diodes an optical indication of the charging state can be realized.

In the circuit shown in **fig. 5.11** two LEDs serve as indicator. Both diodes are dark, if the battery voltage level is below 11.0 V. If the red LED is on, the voltage is between 11.0 and 12.5 V, i.e. the battery has not been charged totally. If the green LED is on–the red one is then switched off–the voltage is higher than 12.5 V, i.e. the battery is either charged to capacity or is being sufficiently recharged whilst the automobile is being driven.

Is the second threshold of 12.5 exceeded, the value of response can be increased from 11 V to 14.8 V by means of a feedback. The first amplifier which was turned off at 12.5 V now reacts again when the voltage exceeds a value of 14.8 V. The resulting third threshold is indicated by both LEDs. If both diodes emit light, the voltage is higher than 14.8 V, i.e. the battery is overcharged. In practice this happens only in the event of a defective voltage regulator.

The LEDs indicate the following situations:

green light	everything is in order
red light	battery is being charged insufficiently or not at all
red and green light	battery is being overcharged

The green LED should therefore always glow during unobstracted driving. The red one, however, should light before the engine is started and during stops, e.g. traffic lights, when the engine is idling, especially if a large part of the electrical load is left switched on.

Occasionally lightning of the red LED during forced stops is not critical unless, e.g. when traffic conditions necessitate much stopping and starting, the recharging time (green light) is too short. In such cases the consumption of energy must be kept to a minimum.

A defect is existent if the green diode remains dark during unobstructed driving. If none of the diodes is lighting before the engine is started, the battery is either already exhausted or a residual charge is present. In the latter case it should be conserved as much as possible for starting.

If both diodes are lighting during unobstructed driving, the battery is overcharged due to a defective regulator. In this case additional electrical loads should be turned on until the defect has been eliminated.

Mode of operation

As reference standard serves a z-diode inserted in a bridge circuit. The bridge resistors are so adjusted, that the following opamps TAA 865 react exactly at the desired thresholds and turn the indicator LEDs on. The opamps operate with a weak feedback in order to achieve definite switching. If the applied battery voltage has such a high level that the threshold with higher value is again already reached or even exceeded, the opamp responsible for the threshold with lower level switches off by the feedback diode BAY 44. Thus the red LED turns off and the green one starts to emit light.

By adjusting the inserted resistor R_3 the first bridge divider can be definitely detuned by the value of the second threshold so as to realize a third threshold. If the battery voltage rises, probably due to a defective voltage regulator, the first opamp reacts again at 14.8 V and both the green and the red LED glow in order to indicate that the battery is being overcharged.

The light dots have such a high intensity that they are visible clearly also at daylight.

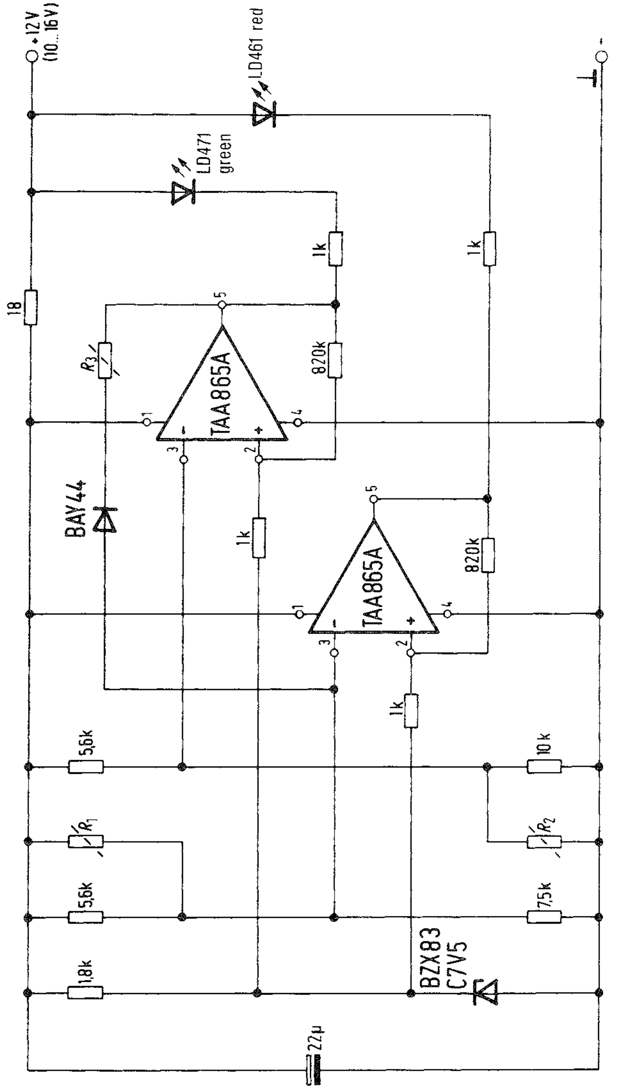


Fig. 5.11

Technical data of charge indicator

Operating voltage	0 to 16 V
Current consumption at	
V_{batt} = 11.0 V	12 mA
V_{batt} = 13.5 V	15 mA
V_{batt} = 15.0 V	30 mA
Thresholds	11.0 V
	12.5 V
	14.8 V
Temp. coefficient	+3 to 6 mV/K
Ambient temperature	−25 to +80 °C

R_1, R_2, R_3 fixed resistors, after individual adjustment.

5.12 Flasher unit for 24 V$_\sim$

Fig. 5.12 shows a flasher unit especially designed for 24 Vac. The frequency is adjustable between 0.5 and 60 Hz with a pulse duty factor of 1 : 1 by means of the 10-kΩ-potentiometer. The minimum (relay)-load is 200 Ω. Two cradle relays in parallel, type V23154-N4720-C112 are projected. The current consumption is 140 mA at 24 V ac.

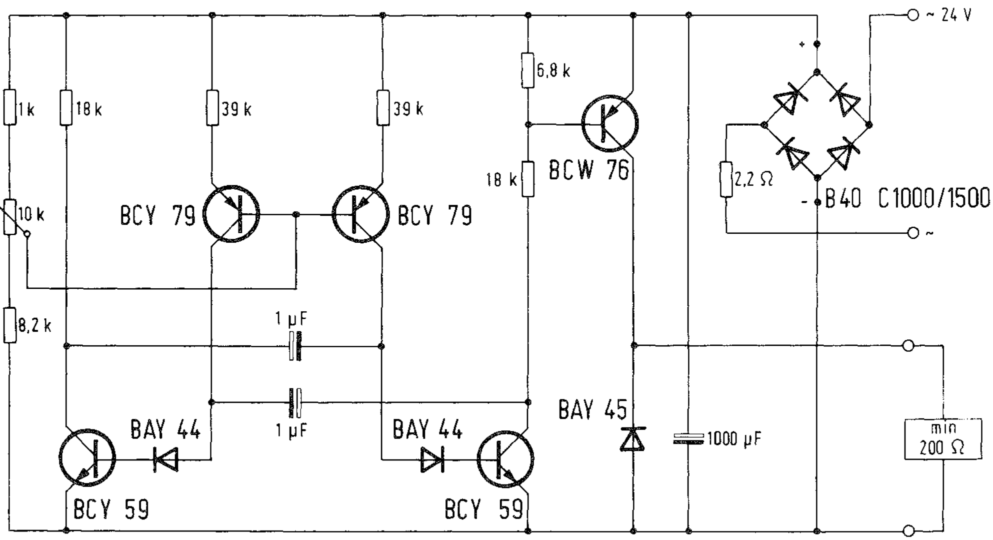


Fig. 5.12

5.13 Electric fence device, battery operated

An electric fence device supplies voltage pulses to a wire fence mounted on insulators. If the fence is touched neither human beings nor animals are to be injured. According to VDE-standards the voltage pulse is to have a value of 2000 V min and not more than 5000 V at a load of 1 MΩ parallel to 10 nF.

The fence is most effective, if the pulse has a value of 2 kV at nominal load of 50 kΩ // 10 nF (standard fence). The pulse interval is specified with 1 sec. ±25%, whereby the quantity of electricity per pulse is not to exceed a value of 2.5 mA sec. The pulse duration is about 2 ms.

The electrical requirements for such a divice are understandably high. The current consumption has to be low, i.e. the device has to have a good efficiency. On the other hand, the current is not to increase essentially, if the output of the device is shorted, interrupted or even capacitively or non-reactively loaded. Besides that the unit has to operate at high ambient temperatures.

The control multivibrator consists of the transistors BCY 58, BCY 78, BSX 45 and additional passive components. The pulse duration is adjusted to 4.2 ms in this example by means of the 250-Ω-potentiometer. The pulse repetition period is set by the 25-kΩ-potentiometer to a value of 1.25 sec. This single-adjustment has to be made very carefully. For the main circuit a transistor type 2N3055 is necessary. The diode SSi B0101, connected in parallel, is required for the inverse current of each pulse. The 22-μF-capacitor clips the voltage peaks to a value of 60 V at the transistor during non-load operation.

In accordance to the permissible power dissipation of the transistor a core of M 65 is sufficient for the pulse transformer, which stores the energy and which must have an air gap of 0.5 mm. The high-voltage turns have to be wound very carefully. The load is coupled to the primary windings by a capacitor of 50 nF in order to avoid a feedback to the transistor 2N3055 when the output circuit is shorted. Instead of the capacitor also a diode can be used with a reverse voltage of 1000 V and a surge current of 100 mA (1N4007). A glow lamp indicates whether the device operates or not. The supply voltage is 8 V. This is the voltage normally available from a 9-volt-battery. Although an average current of only 16 mA is flowing, a current pulse with a value of 5 A is generated during the switching time of the transistor 2N3055. Therefore the internal resistance of the battery has to be reduced by a capacitor in parallel with a value of 2.5 to 5 mF.

Technical data:

Operating voltage	V_o	8 V
Average current	$I_{battery}$	16 mA
Collector peak current	I_C	7 A
Pulse interval	T	1.25 sec
Pulse duration	t_1	4.2 ms
Pulse separation (= fence pulse duration!)	t_2 (50 kΩ // 10 nF)	2 ms
Output voltage	V_a	
Load 50 kΩ//10 nF		2.4 kV
Load 1 MΩ//10 nF		3.7 kV
Non-load operation		6 kV
Max. ambient temperature		60 °C

Transformer

M65 dyn. sheet IV
air gap of 0.5 mm
n_1 = 50 turns 1.0 CuL
n_2 = 5000 turns 0.12 CuL

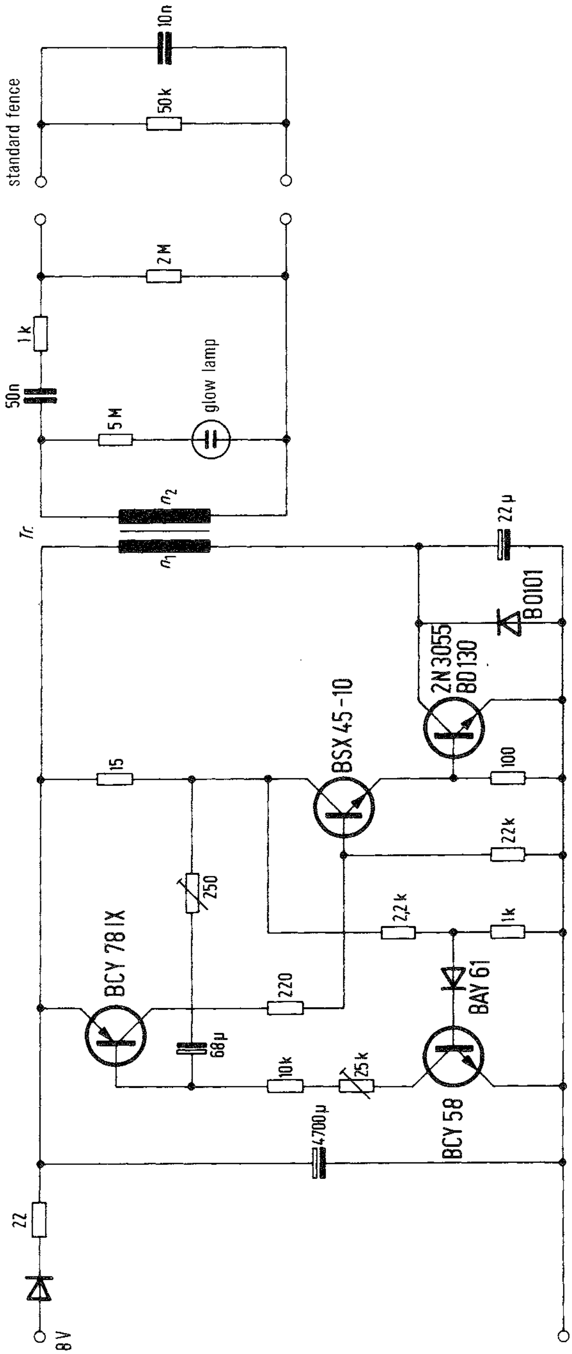

standard fence
10n
50k
2M
1k
50n
5M
glow lamp
Tr.
n_1
n_2
22µ
BD101
2N3055
BD130
BSX 45-10
15
100
22k
250
2,2k
1k
BCY 78 IX
220
BAY 61
68µ
10k
25k
BCY 58
4700µ
22
+8V

Fig. 5.13

6. Power supply circuits

6.1 Parallel-control circuits

Parallel-controlled circuits operate as self-controlled, variable resistors, connected in parallel to the load impedance (parallel loads). They react extremely fast and also control immediately pulses and very short mains break-downs, resulting from strong loads. These devices are preferably used in TV receivers, which have a B-class operated audio output stage. Without any parallel control the picture width is influenced inconveniently by the rhythm of speech and music. However not only in TV receivers a parallel control circuit is advantageous, but there are also a lot of applications requiring such a design.

The parallel control circuit can also be described as a "z-diode booster", which offers, however, the great advantage, that the power dissipation of the control transistor can be reduced to a quart of that of a z-diode representing the same function. Thus the collector resistor can take the total parallel-load when the transistor is switched on. Supposing that half of the voltage is available at the collector, only half of the current flows through the transistor, power dissipation of which is only a quart of the total power consumption of the parallel load. The circuits 1 and 2 are proportioned for a parallel load of $\leqq 6$ W. In many cases the former is sufficient. It is characterized by a remaining control voltage of < 250 mV. The circuit no. 2 consists of two stages and improves the voltage control to about 20 to 50 mV. The small elaborateness of only one transistor and one resistor is advantageous in many cases.

The circuits of **fig. 6.1** and **6.1.1** are designed for fixed output voltages. The resistance of R_v is determined on the control range, on the value of the supply voltage and on its fluctuation. The maximum range of power control is determined by the resistance of R_p (control resistor).

The circuits of **fig. 6.1.2** and **6.1.3** are dimensioned for a power of 15 or 30 W. The output voltage is adjustable in a range of 24 to 35 V, for instance. As it can be seen the circuit of **fig. 6.1.3** employs only one transistor, the Darlington-transistor BD 675.

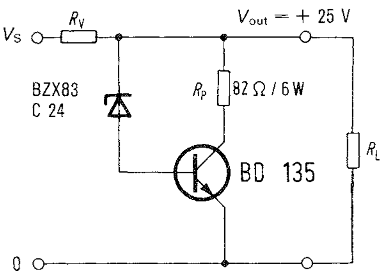


Fig. 6.1

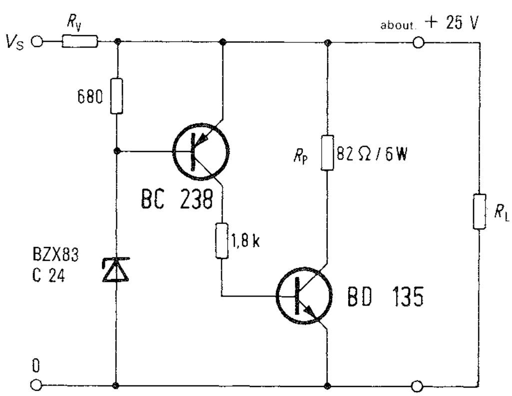


Fig. 6.1.1

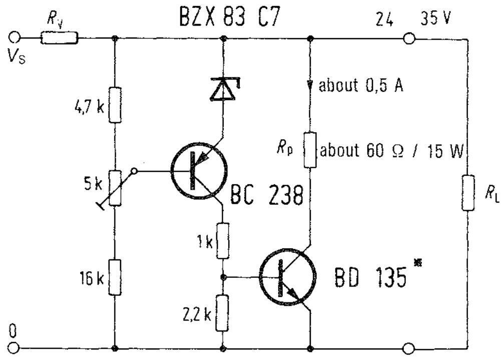


Fig. 6.1.2

* heat sink 10 K / W

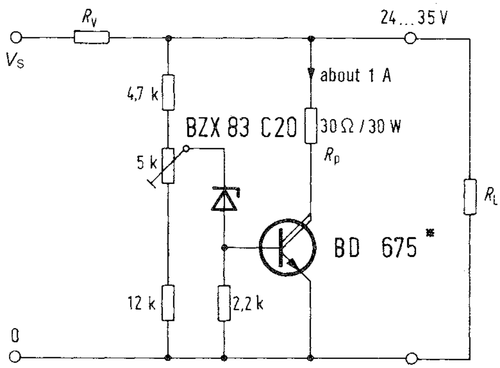


Fig. 6.1.3

* heat sink 5 K / W

6.2 Voltage regulator ± 15 V/5 A

The **fig. 6.2** shows the circuit of a regulated power supply for ±15 V and 5 A. The output voltages are adjustable between 12 and 17 V.

A tape-wound core transformer is used. It offers a better power-to-volume ratio than conventional ones with laminated cores. The voltage control is achieved by two series transistors, connected in parallel, and by the opamp TAA 761, which acts as control amplifier. For the negative voltage the ground potential serves as reference level for the desired-to-actual value comparison.

The voltage is adjusted by the potentiometers P_1 and P_2, whereby the centre tap of P_2 is set firstly to 0. Then both output voltages can be adjusted symmetrically through P_1 (range between 12 V and 17 V, for instance).

NPN power-transistors are used as series-control components for the positive as well as negative voltage. Since two transistors 2 N 3055 have to be connected in parallel for each output voltage, 0.22-Ω-resistors are inserted in their emitter leads to achieve a symmetrical load splitting.

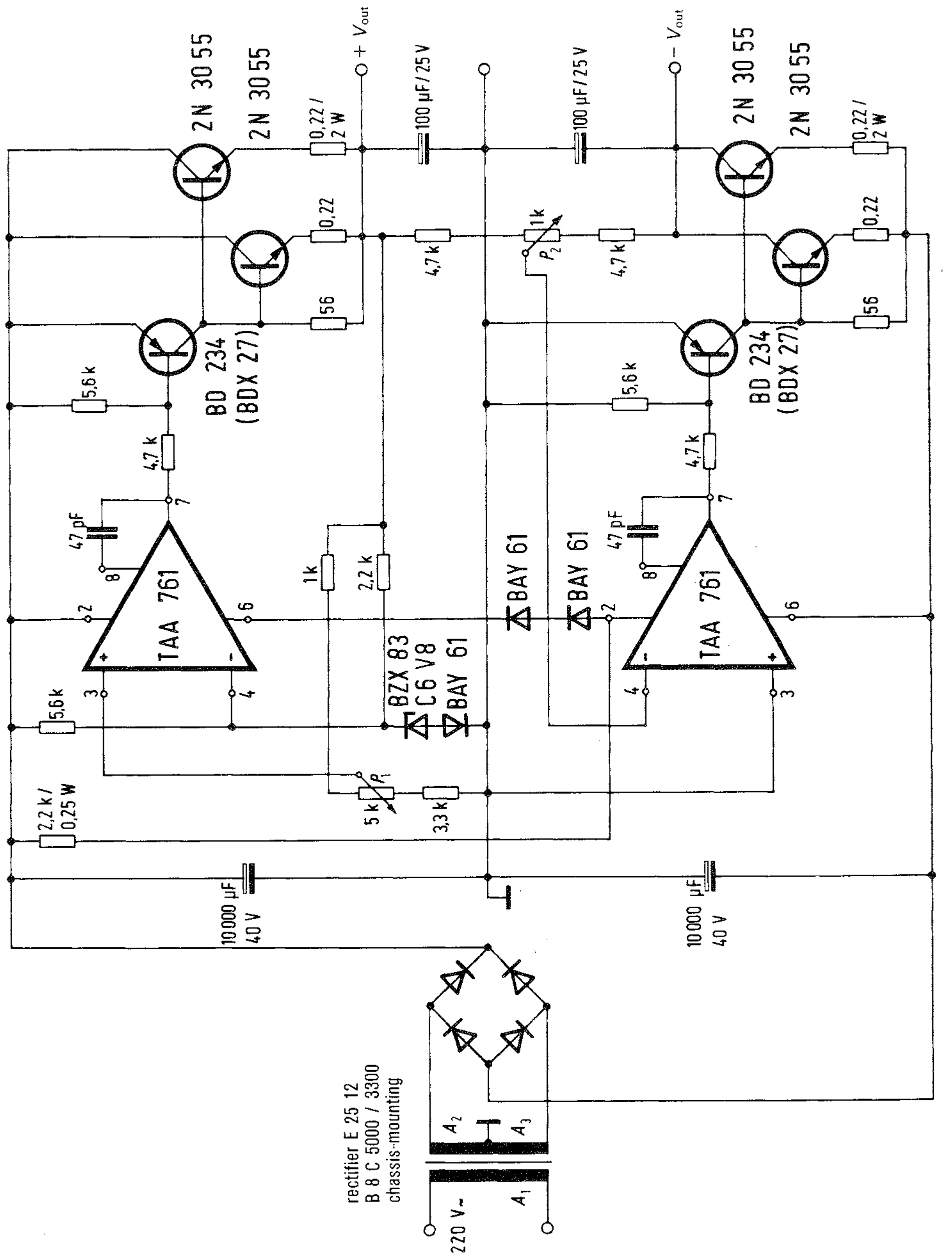

2N 3055
2N 3055
2N 3055
2N 3055
0,22 / 2 W
0,22 / 2 W
0,22
0,22
56
56
+ V_{out}
− V_{out}
100 µF/25 V
100 µF/25 V
4,7 k
4,7 k
1 k
P_2
BD 234 (BDX 27)
BD 234 (BDX 27)
5,6 k
5,6 k
5,6 k
4,7 k
4,7 k
47 pF
47 pF
TAA 761
TAA 761
1 k
2,2 k
BAY 61
BAY 61
BZX 83 C6 V8
BAY 61
P_1
5 k
3,3 k
2,2 k / 0,25 W
10 000 µF 40 V
10 000 µF 40 V
rectifier E 25 12
B 8 C 5000 / 3300
chassis-mounting
220 V~
A_1
A_2
A_3

Fig. 6.2

Technical data:

Mains voltage	220 V/±15%/50 Hz
Output voltages	±15 V (adjustable from 12 to 17 V)
Max. output current	5 A each
Max. ambient temperature	50 °C

Mains transformer

Tape-wound core	2×SE 130 a
Primary windings (220 V)	n_1 = 490 turns/d = 1.0 mm ∅
Secundary windings	$n_2 = n_3$ = 50 turns/$d_2 = d_3$ = 1.8 mm ∅
Ordering code	B71725-A130-A2

Thermal resistance of heat sinks

for each transistor 2 N 3055	$R_{th} \leqq 2.5$ K/W
for each transistor BD 234	$R_{th} \leqq 23$ K/W or
for each transistor BDX 27	$R_{th} \leqq 38$ K/W

6.3 Sinus/trapezium-switch mode power supply 220 V/2 × 30 V/1,6 A with mains separation

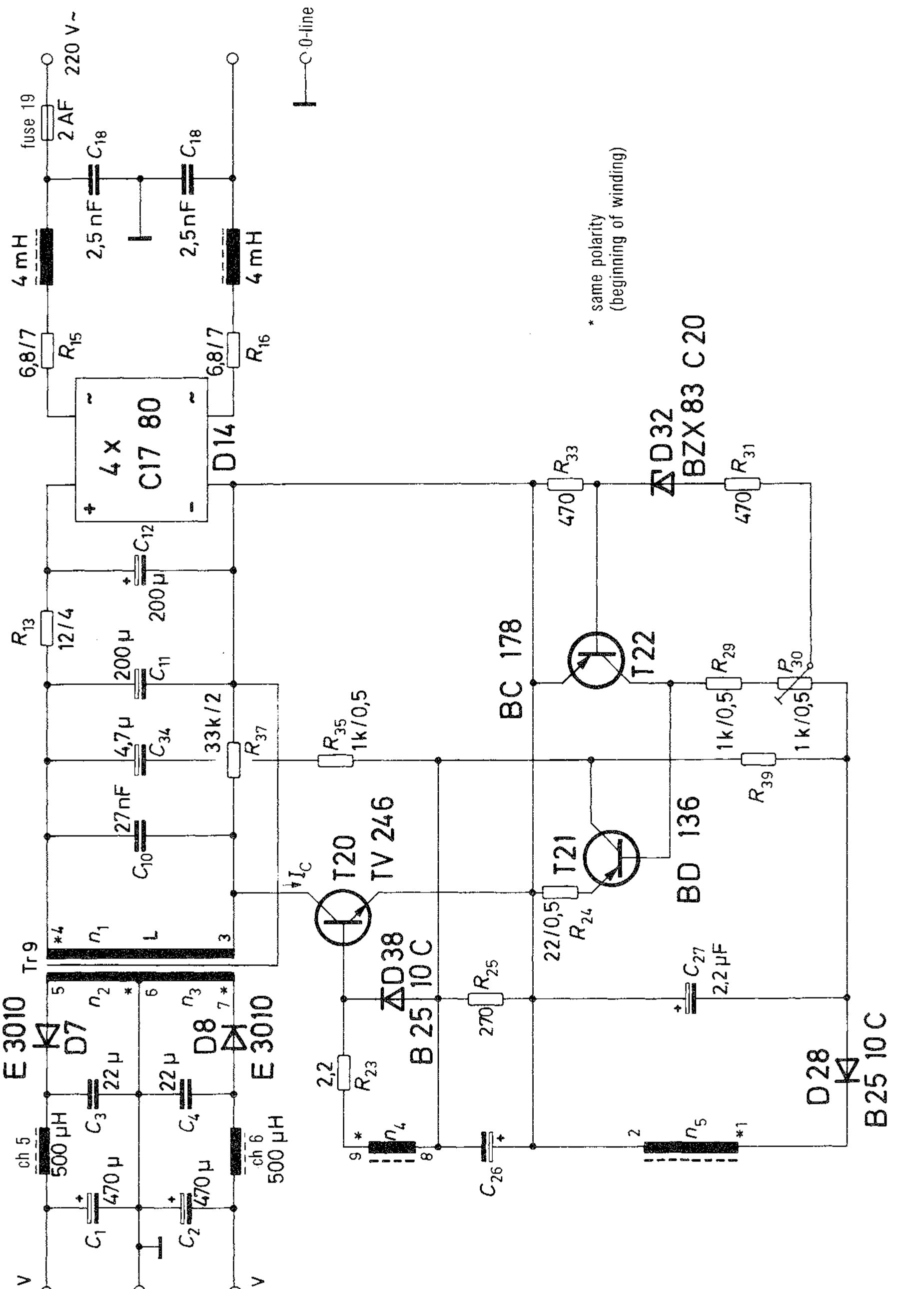
High-frequency power supplies are essentially advantageous as against conventional ones, 50-Hz-operated, particularly in the case when a constant output voltage is required. This kind of power supplies has already been described fundamentally in Design examples of Semiconductor Circuit, edition 1974.

Function of the circuit shown in **fig. 6.3**

The operating voltage V_B for the switching transistor T_{20} is available across the capacitor C_{12}. It is produced from the mains voltage through the four diodes C1780. The transformer Tr_9 (L) and the capacitor C_{10} realize a resonant circuit with a resonance frequency of about 20 kHz. The feedback voltage for the base is supplied via the winding n_4. The negative half-wave is clipped by diode D_{38}. Thus only the half of the peak-to-peak voltage of n_4 is applied as reverse voltage to the base of transistor T_{20}. The operating voltage for the control transistors is generated by rectifying the voltage across the winding n_2, whereat the transistor T_{22} is controlled by the diode D_{32}.

The exact output voltage is adjusted through potentiometer P_{30}. Through the control current of T_{22} and T_{21} a differently biased base voltage is achieved at C_{26}, whereby positive currents of half-waves with variable duration are supplied to the base of T_{20}. Thus the switching time and the collector peak-current are controlled. The output circuit consists of the secondary windings n_2/n_3 of Tr_9, the diodes D_7 and D_8 as well as of the components C_3, C_4, ch_5, ch_6, C_1 and C_2. It supplies the rectified and filtered output voltages.

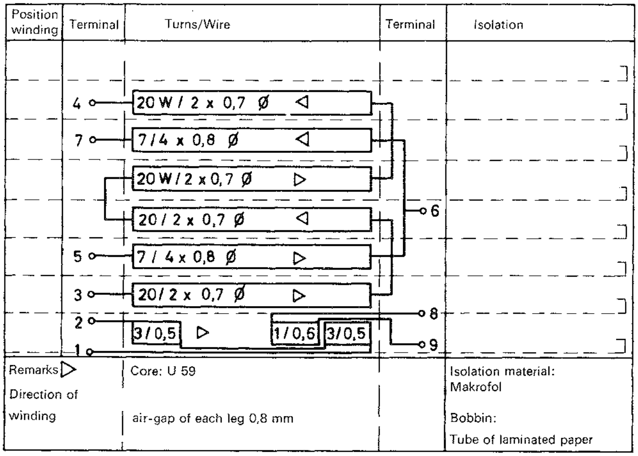
The power supply shown in **fig. 6.3** is essentially characterized by a resonant circuit ($L-C_{10}$). The oscillation frequency depends on load and on operating voltage. The shape changes from sinus to trapezium. Only a resonant circuit in combination with the biased base control achieves an "ideal" switching behaviour. The control of the base starts not before the collector voltage has reached its zero value. In the following charging period of the transformer inductance L the collector current I_C rises continuously from a negative (inverse) value to a peak current determined by the control circuit. During the cut-off period of the current, the collector current



220 V~
fuse 19
2 AF
C_{18}
2,5 nF
4 mH
0-line
6,8/7
R_{15}
R_{16}
4 x
C17 80
D14
* same polarity
(beginning of winding)
D32
BZX 83 C 20
R_{33}
470
R_{31}
470
R_{13}
12/4
C_{12}
200 µ
200 µ
C_{11}
BC 178
T22
R_{29}
1k/0,5
P_{30}
1 k/0,5
4,7 µ
C_{34}
33k/2
R_{37}
R_{35}
1k/0,5
R_{39}
27nF
C_{10}
I_C
T20
TV 246
T21
BD 136
22/0,5
R_{24}
Tr 9
n_1
n_2
n_3
E 3010
D7
D8
E 3010
D38
B 25 10 C
R_{25}
270
C_{27}
2,2 µF
D 28
B 25 10 C
2,2
R_{23}
n_4
n_5
C_{26}
ch 5
500 µH
ch 6
500 µH
C_3
22 µ
22 µ
C_4
470 µ
C_1
470 µ
C_2
+ 30 V
0
- 30 V

Fig. 6.3

Winding data of transformer Tr_9



is decreased to zero before the collector voltage can increase at the switching transistor (the capacitor C_{10} intends to keep its voltage, thereby the current has enough time to decrease).

By dc bias-variation of the transistor base the feedback ac bias of the base is controlled, whereby the turn-on time of the transistor is varied. Through this principle a simple dc-control is possible, whereby a two-stage dc amplifier is used as a control amplifier, because a better stabilization of the output signal with less hum is achieved.

The mains voltage (220 V_{rms}) is rectified by a bridge circuit.

The circuit is proportioned in the way that the transistor does not operate in the critical overload range of the characteristics family. There are only the following situations, current but no voltage and voltage but no current. At overload or total load the max. voltage is less than 130 V at a moment, where the collector current is zero. After that the voltage rises to $V_{CEV} \rightarrow 700$ V. At no-load operation the max. voltage is even lower than 40 V at a current downward-acting control.

This nearly ideal behaviour is only achievable by a resonant circuit in combination with the described delayed control. This principle of operation offers additionally the advantage that the transformer has not to transmit square-wave voltages, i.e. it is easily to realize and an extremely low magnetic leakage is not required, especially if transistors with higher reverse voltages are used.

In principle the variations of collector current and voltage at constant load and operating voltage V_B is shown in **fig. 6.3.1**. The curve 1 represents a low load, no. 2 is for nominal load and no. 3 applies for full load. The discharge voltage (350 V) is constantly controlled (indirectly) at the inductor L. Duration as well as amplitude of the L-charging current (I_C) vary in dependence on the operating voltage and the load. Duration and amplitude of the discharging current (I_D) which flows via the diode D_7 or D_8, are determined by the load. Curve no. 3 indicates the failure of oscillations when a load circuit is shorted.

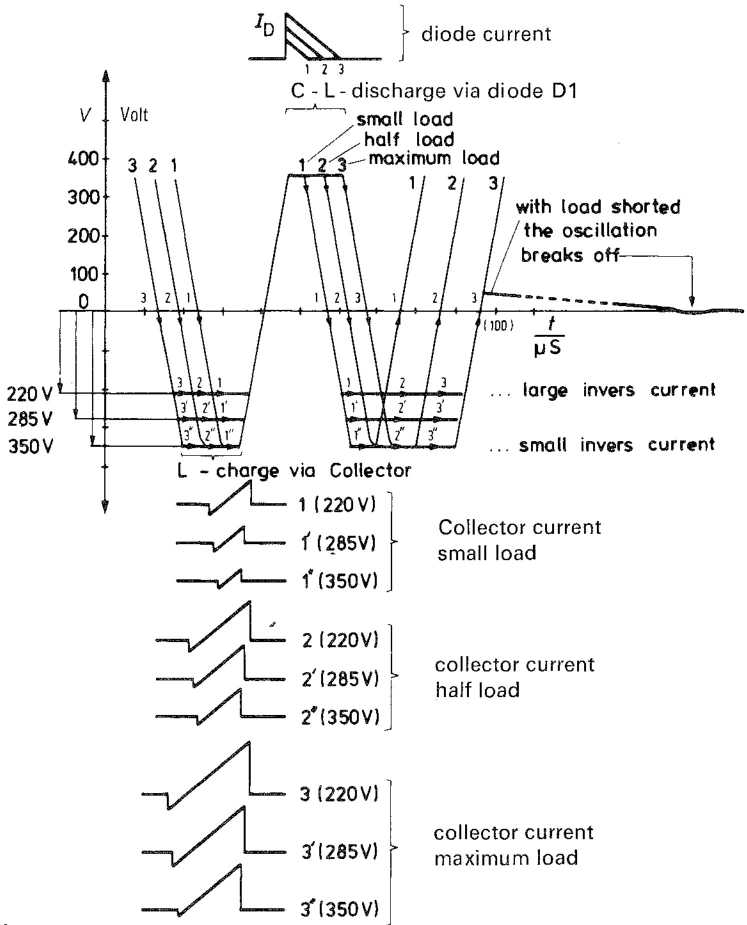


Fig. 6.3.1

6.4 Switch-mode power supply with optoelectronic coupler and mains separation

The operation principle of the circuit shown in **fig. 6.4** is the same as that of **fig. 6.3** with the only exception that the controlled variable is not directly taken off from the load circuit but indirectly. Thus a better regulation of mains or load variations is achieved.

The optoelectronic coupler CNY 17, specified for an insulation voltage of 2.5 kV, supplies the amplified signal directly to the control transistor T_3, connected to the switching transistor T_4.

The control voltage of the z-diode is amplified by a transistor T_1 infront of the optoelectronic coupler in order to get sufficient current and voltage variations of the coupler LED. The output voltage is adjustable in a small range through potentiometer P.

Technical data:

Mains voltage	220 V/50/60 Hz±10%
Output	2×30 V/1.6 A

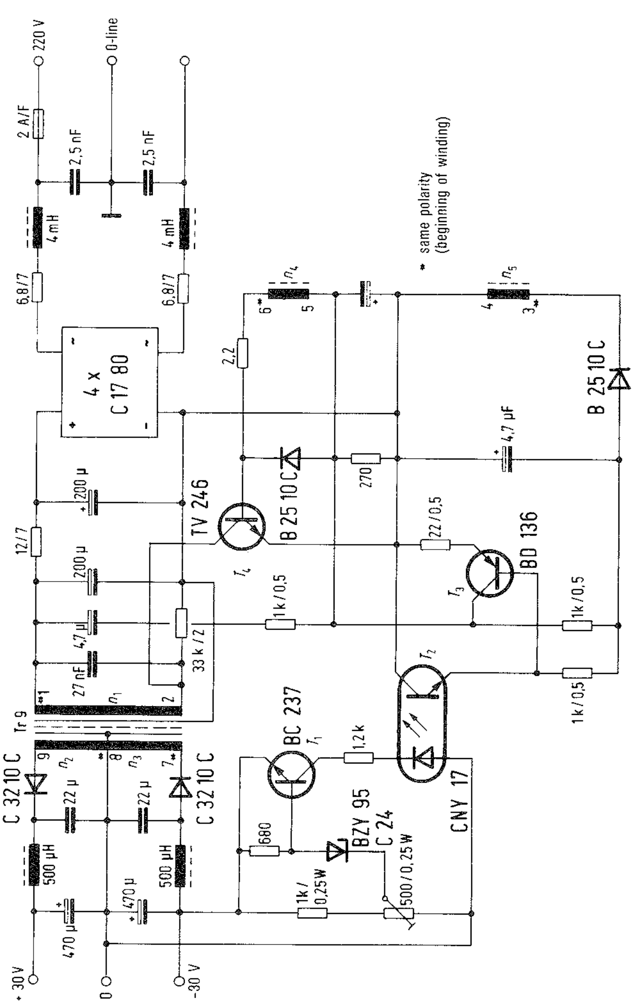
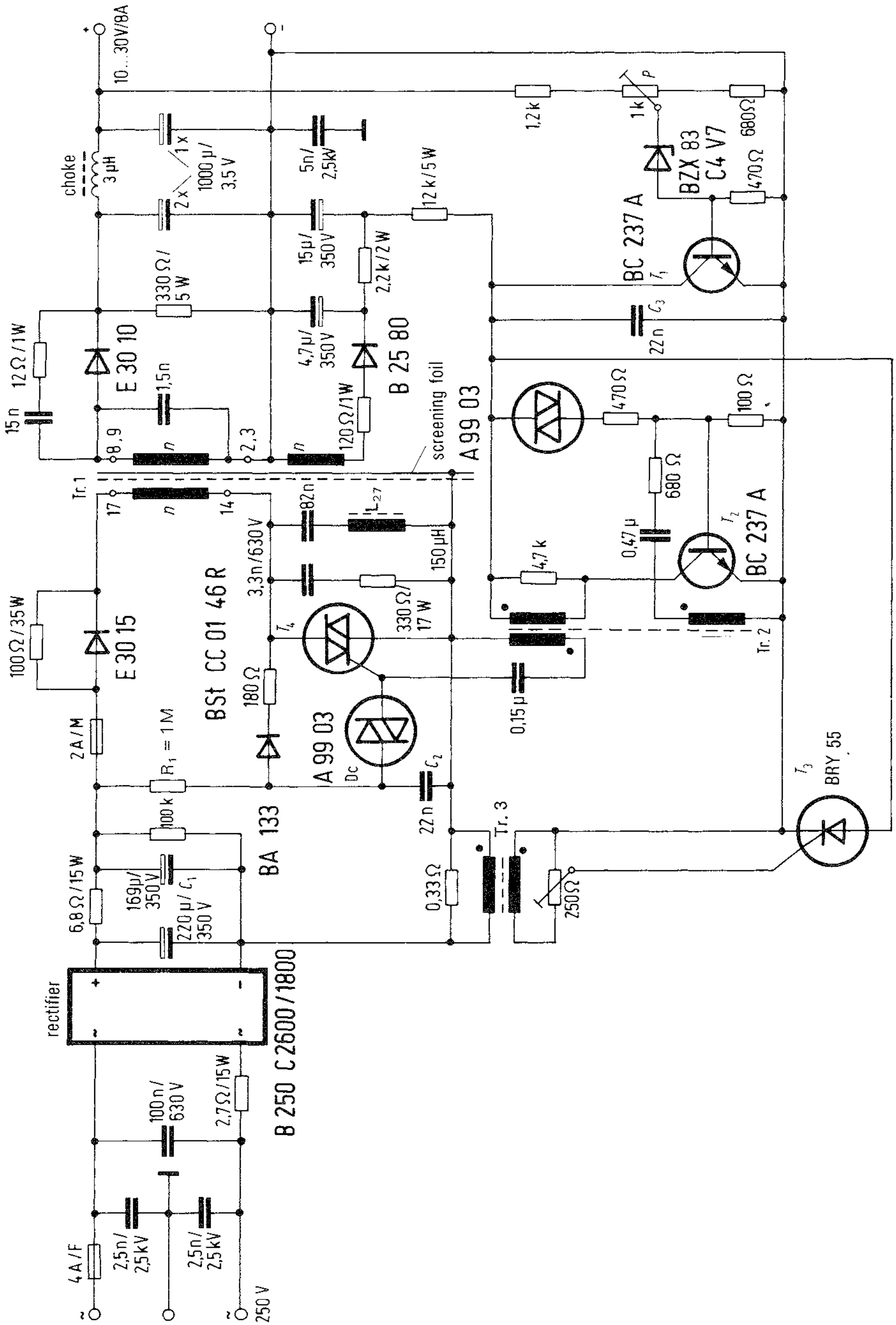


Fig. 6.4

6.5 Thyristor switch-mode power supply with an output voltage adjustabe in a range of 10 to 30 V / 8 A

The switch mode power supply described in the following **(fig. 6.5)** can be considered as a very safe one. It features a mains separation and an output voltage adjustable in the range of 10 to 30 V at a load current of 8 A. Conventional voltage regulator devices with heavy mains transformer and high-power dissipated series control networks can be replaced by this power supply. If a greater control range of the output voltage is required, then this has to be arranged on the secondary side of the transformer. A fast switching thyristor, type BSt CC01 46R, is used. On account of its internal reverse-current diode with high power dissipation, this thyristor can be considered as an integrated circuit.



10...30V/8A
choke
3 µH
2 x
1 x
1000 µ/
3,5 V
5n/
2,5kV
15µ/
350 V
4,7µ/
350 V
330 Ω/
5 W
2,2 k/2 W
12 k/5 W
1,2 k
1k
P
680Ω
BZX 83
C4 V7
470Ω
BC 237 A
T_1
C_3
22 n
12 Ω/1W
15 n
E 30 10
1,5n
B 25 80
120Ω/1W
8, 9
2, 3
n
screening foil
A 99 03
470 Ω
100 Ω
680 Ω
0,47 µ
T_2
BC 237 A
4,7 k
Tr. 1
17
14
82n
L_{27}
150µH
3,3n/630 V
330 Ω/
17 W
BSt CC 01 46 R
T_4
100Ω/35W
E 30 15
180 Ω
Tr. 2
0,15 µ
2A/M
A 99 03
Dc
C_2
R_1 = 1M
100 k
BA 133
22 n
Tr. 3
T_3
BRY 55
6,8 Ω/15 W
169µ/
350 V
C_1
220 µ/
350 V
0,33 Ω
250Ω
rectifier
B 250 C 2600/1800
100 n/
630 V
2,7 Ω/15 W
2,5n/
2,5 kV
2,5n/
2,5 kV
4 A/F
250 V

Fig. 6.5

At the transformer a nearly rectangular oscillation is generated (about 20 kHz). Its peak value corresponds to the rectified voltage at the electrolytic capacitor C_1. The start of oscillation with relatively low frequencies is achieved through the diac Dc and the starting-diac-generator, which supplies the first pulses to the transistor T_4. The controlled variable is picked up at the potentiometer P. It is compared with the voltage of the reference diode and applied to the control transistor T_1, which controls not only the charging time of C_3, but also the frequency and the duty factor by means of the diac generator. The rectangular control voltage is supplied to the switching thyristor T_4 via the transformer TR 2. Through the thyristor T_3 the beginning of the over-current control at the output is set.

The stability of the output voltage is about 1.5% in the range of full load to no load. An efficiency of 65% is achievable with this device.

Technical data:

Mains voltage (±10%)	220 V/50 Hz
Output voltage	10 to 30 V/8 A
Regulation at mains variations (±10%)	±0.3%
Regulation at load variations (0 to 100%)	−1.5%
Hum	<1%

6.6 Switch-mode power supply for halogen projector lamp

With the power supply described in the following the heavy mains transformer, dimentioned for load of 150 W, is replaced by a small and light ferrite transformer. It oscillates at about 20 kHz and employs the fast switching thyristor BSt CC01 46. The operation principle of this circuit has already been described in Design Examples of Semiconductor Circuits, editions 73 and 74. The projector lamp is connected to the secondary side of the transformer directly, i.e. no rectification is used **(fig. 6.6)**. Therefore one diode with heat sink, one or two electrolytic capacitors and other components can be economized at least.

It seems to be possible to use this power supply also for a 250-W-lamp, if it is dimensioned accordingly.

Technical data:

Mains voltage	220 V (±10%)
Halogen lamp	15 V/10 A

6.7 Radio interference suppression of switch-mode power supplies

On principle the **figures 6.7 a** to **d** demonstrate the radio interference situations which will be found in switch-mode power supplies. **Fig. 6.7 a** shows the transformer being responsible as well for mains separation as for transmitting. If the circuit of the primary side includes a transistor or a thyristor which oscillates at higher frequencies, a square-wave oscillation is generated on the primary as well as on the secondary side. If the edges of this oscillation are very steep, a broad frequency spectrum is achieved. **Fig. 6.7 b** shows primary and secondary windings including a square-wave generator each. Both generators are coupled by the winding capacitance. Although the capacitors C_1 and C_2 shorten partially the primary and secondary interferences, both generators have an effect against the mains as well as against the load via the winding capacitance C_w. Something like an open dipol is created, whereby its generator is situated in the middle **(fig. 6.7 c)**. This 'antenna-effect' can be reduced by making a connection to ground or to the neutral line. Thus the 'cold ends' of the primary and secondary windings are combined (shorted) and connected to ground.

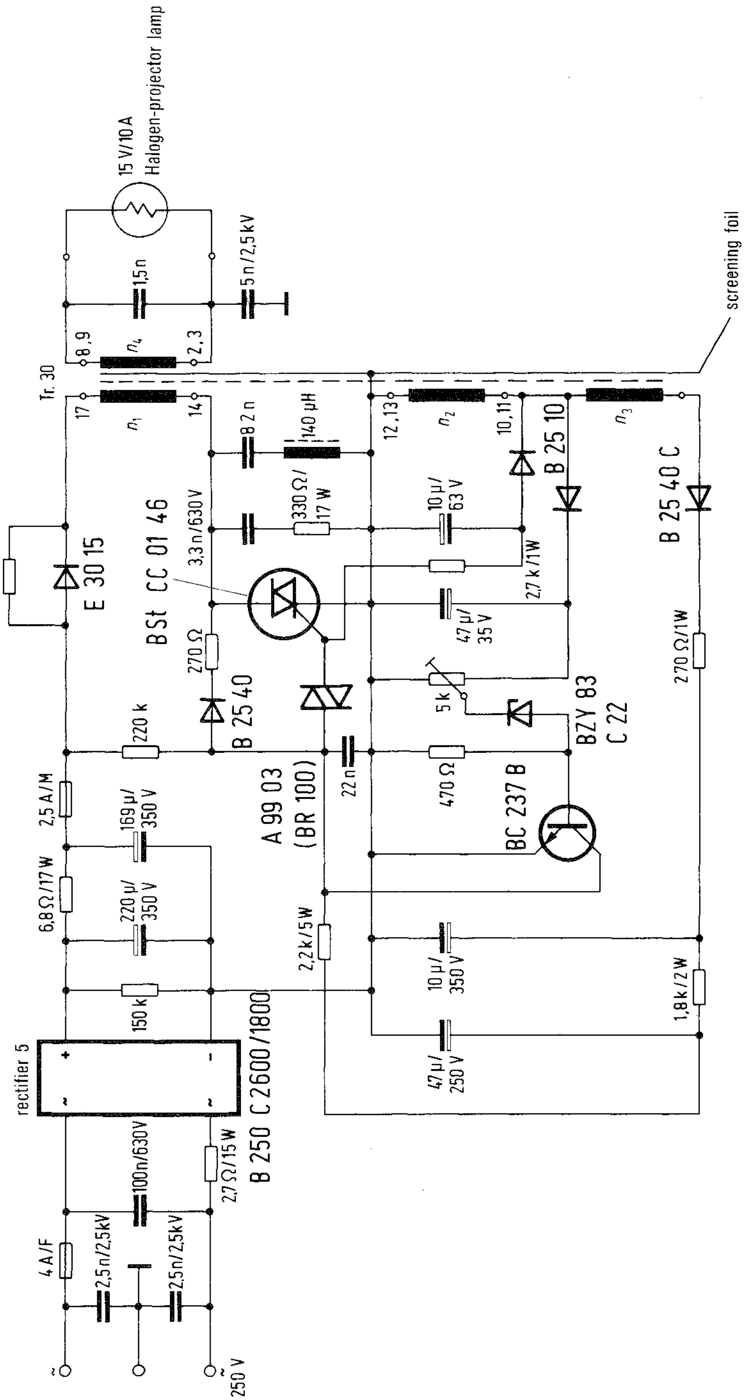

15 V/10 A
Halogen-projector lamp
1,5 n
5 n/2,5 kV
8,9
n_4
2,3
Tr. 30
17
n_1
14
8 2 n
140 µH
12,13
n_2
10,11
n_3
screening foil
B 25 10
B 25 40 C
47 Ω/35 W
E 30 15
3,3 n/630 V
330 Ω/
17 W
10 µ/
63 V
BSt CC 01 46
2,7 k/1W
47 µ/
35 V
270 Ω
B 25 40
5 k
BZY 83
C 22
270 Ω/1W
220 k
22 n
470 Ω
A 99 03
(BR 100)
BC 237 B
2,5 A/M
169 µ/
350 V
6,8 Ω/17 W
220 µ/
350 V
2,2 k/5 W
10 µ/
350 V
1,8 k/2 W
150 k
47 µ/
250 V
rectifier 5
B 250 C 2600/1800
100n/630V
27 Ω/15 W
4 A/F
2,5 n/2,5kV
2,5n/2,5kV
~
~
250 V

Fig. 6.6

This measure improves the radio interference suppression essentially, but it is not sufficient in most cases. Often it is not practicable to ground the primary or secondary windings. In such cases a screening winding is helpful, whereat the secondary side of the transformer has to be grounded symmetrically or non-symmetrically. If this secondary grounding is impossible, then the only measure is to screen both the secondary and the primary side **(fig. 6.7d)**.

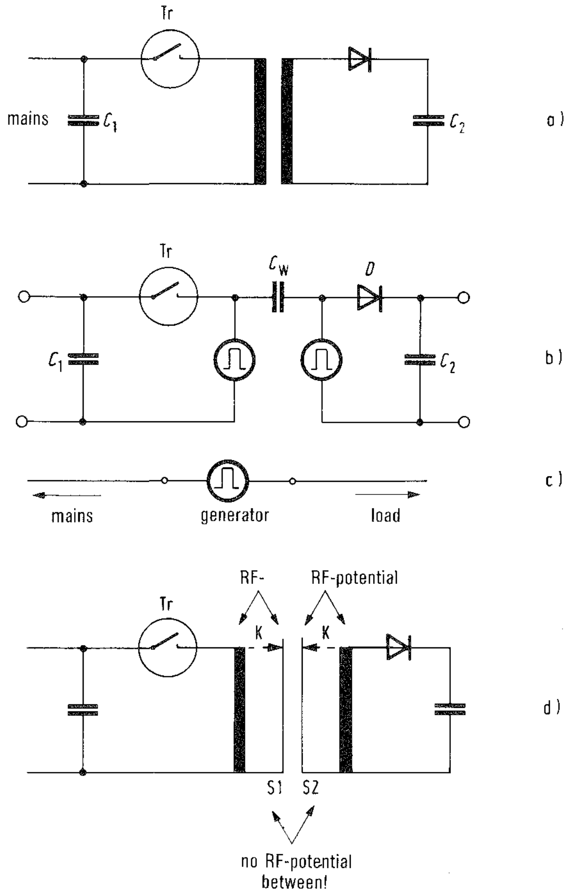


Fig. 6.7

The functional operation of the double-screening is shown in **fig. 6.7d**. Essentially a rf short-circuit is produced for each screening, thus there is no rf-potential difference between both. This means, that radio interferences are generated only by the short connection between transformer and the diode. If the 'hot end' however, is placed inside of the screening and the 'cold end' outside, the interference suppression is additionally improved. But it has to be considered, that the screening foils produce additional losses, i.e. they have to be thin and the screening windings have not to have any short circuit. Both screenings are insulated according to the standards. A primary and secondary grounding improves the suppression again. It has to be mentioned that additional, in some cases essential, radio interferences are generated by the diodes. These, however, have to be suppressed by suitable RC-networks. Overshoots at the transformer have to be damped through appropriate RC-circuits. Its in- and output have to be provided with suitable chokes and pulse-proof capacitors. In some cases a screening of the total device cannot be avoided.

7. Digital circuits

7.1 Level interface between TTL, LSL, and MOS logic systems

Nowadays digital technology uses TTL, LSL and MOS circuits, whereas each of them, in view of its peculiar nature, has a specific field of applications. In electronic control systems one often tries to utilize the advantage of two or even of all three systems of these families. However, these techniques are not compatible without any level transformation and the user is confronted with the problem of finding the simplest level interface. A system with input periphery, central control logic and output periphery is shown in **fig. 7.1.1** as a typical application.

The input periphery has the task of removing the noise from the input signals. The LSL system is best suited to meet this demand for great dynamic noise immunity.

The central control logic is usually characterized by two features: it offers a higher operation speed than the periphery unit and it has a more complex logic system. Operating speed permitting, this part, even in its most complex form, can be easily integrated into a single MOS-circuit. For higher operating speeds the standard TTL-circuits are favoured.

In most cases a power stage is connected to the output periphery, since power drivers are usually required. In this field a large variety of TTL and LSL-drivers is available.

Fig. 7.1.1

I Input periphery
II Central control logic
III Output periphery
LT Level interface

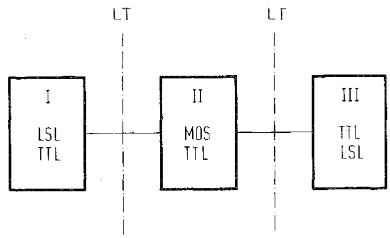


Table 1

		TTL	LSL	MOS-HV	MOS-LV	CMOS
V_0	V	0	0	–	–	0
V_S	V	+5	+12 to +15	–	–	+5 to +15
V_{SS}	V	–	–	0	0	–
V_{DD}	V	–	–	−13	−5	–
V_{GG}	V	–	–	−27	−10 to −15	–

Input and output characteristics of TTL, LSL and MOS-circuits

In view of various voltage supply ranges and the fact that the bipolar techniques are characterized by current-extracting inputs, the different logic families are not directly compatible. Therefore a knowledge of the input and output conditions of the individual circuits is necessary for designing and dimensioning the interface.

Table 1 shows the typical ranges of supply voltages. Compared to the reference level V_0 in TTL and LSL systems, and V_{SS} in MOS circuits, the bipolar technique uses positive supply voltages, whereat the MOS technique requires negative ones. There are two MOS techniques: the high-voltage technique (MOS-HV)·and the low-voltage one (MOS-LV). In addition the complementary technique CMOS, becomming more and more popular for standard applications, has to be named. Due to their favourable supply and threshold voltages, the MOS-LV circuits can easily be matched to TTL circuits. Depending on whether the load is driven saturated or unsaturated, it has in addition to the reference level V_s either one external supply connection V_{DD} or two, V_{DD} and V_{GG}. Using the "saturated" circuit technique the supply voltage may vary between −10 and −28 V and its fluctuation can be specified between ±5% and ±15% in general.

a TTL
b LSL
c MOS with saturated load transistor

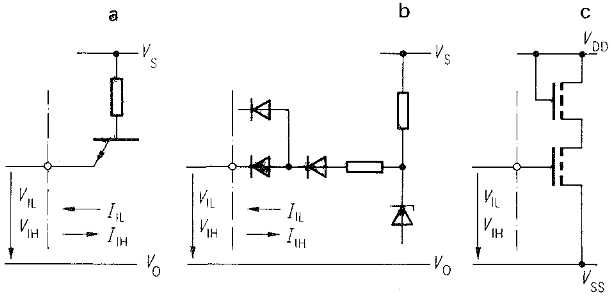


Fig. 7.1.2

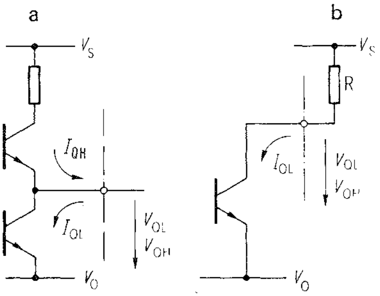
In **fig. 7.1.2** the typical input circuits are shown and in table 2 the corresponding input guiding data are given. The essential difference is that at bipolar inputs a considerable current flows during L-state, while at MOS-circuits the input current is negligibly small, i.e. both stages have a high impedance.

Table 2
Guiding data refered to $V_0 = 0$ and $V_{SS} = 0$

		TTL	LSL	MOS-HV	MOS-LV	CMOS
Input current I_{IL}	mA	$\leqq 1.6$	$\leqq 1.5$	–	–	–
Input current I_{IH}	μA	$\leqq 40$	$\leqq 1$	–	–	–
Input voltage V_{IL}	V	$\leqq 0.8$	$\leqq 4.5$	$\leqq -10$	$\leqq -6$	$< 0.3\,V_S$
Input voltage V_{IH}	V	$\geqq 2.4$	$\geqq 7.5$	$\geqq -2$	$\geqq -1$	$> 0.7\,V_S$
Typical input threshold V_T	V	≈ 1.4	≈ 5.5	≈ -3.5	≈ -2	$\approx 0.5\,V_S$
Dynamic input impedance						
R_{IL}	Ω	$\approx 4\times10^3$	$\approx 10^4$			
R_{IH}	Ω	$\approx 2\times10^6$	$> 10^7$	$> 10^8$		
R_{ILH} or R_{IHL}	Ω	$\approx 1\times10^3$	$\approx 6\times10^3$			
Input capacitance C_I	pF	< 5				

Fig. 7.1.3 shows variants of the output stages. As in TTL and LSL systems push-pull as well as open output circuits are used with MOS-systems. The push-pull output offers a low impedance in both states, while the open output circuit is favoured not only for level interface but also for logic linkage of wired-AND and wired-OR. A basic difference between bipolar and MOS outputs is the fact that in TTL and LSL systems the current can flow only in one direction (I_{QH} flows out, I_{QL} flows into the output); while in MOS-systems both directions are possible for I_{QH} as well as for I_{QL}. As to the output data shown in table 3 it has to be noted, that MOS outputs, particularly at special-order circuits, have to be designed always as highly resistive as

possible in order to save space. Interfacing MOS-outputs and bipolar inputs, it has to be considered that the voltage drop caused by the bipolar input current I_{IL} flowing through the MOS output resistor does not exceed the permissible V_{IL}-voltage at the bipolar input.



a TTL and LSL: push pull circuit
b TTL and LSL: open collector
c MOS:

① open drain
② Single-ended circuit with diffused resistor
③ Single-ended circuit with saturated transistor
④ Single-ended circuit with non-saturated load transistor
⑤ Push-pull circuit

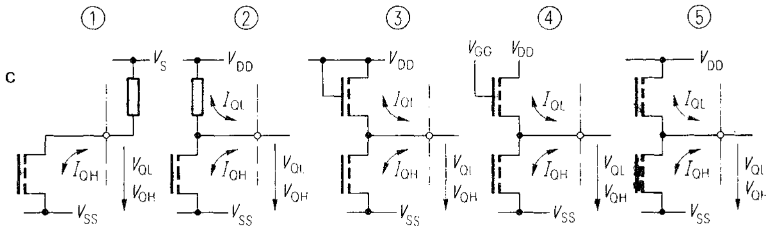


Fig. 7.1.3

Table 3

Guiding data for the output circuits of **fig. 7.1.3**, refered to typical supply voltages with $V_O = 0$ and $V_{SS} = 0$

		TTL		LSL		MOS				
		a	a	b	b	①	②	③	④	⑤
Output current I_{QL}	mA	>16	>16	>15	>15	–	<0.5	<0.5	<1	<2
Output current I_{QH}	mA	>10	–	>7	–	<10		typ. <3		
Output voltage V_{QL}	V	<0.4	<0.4	<1.7	<1.7	< −10 at HV		< −3 at LV		
Output voltage V_{QH}	V	>2.4	–	>10	–	> −2 at HV		> −1.5 at LV		
Short-circuit current I_K to 0	mA	≈25	–	≈15	–	–	<4	<10		*
Output impedance R_{QL}	Ω	≈15	≈15	≈15	≈15	–	>300	10^3	>300	>100
Output impedance R_{QH}	Ω	≈120	–	≈500	–	>100				

* to 0 is not permitted

Examples of level interface

The examples explained here cover most cases of interface. It has to be noted that the gate-level transformers have multiple inputs and they can be included to the corresponding logic complex. Besides the level interfacing they can also perform logic functions (double-input linkage, wired-AND, wired-OR).

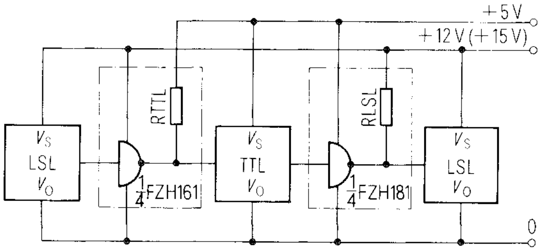


Fig. 7.1.4

LSL – TTL – LSL **(fig. 7.1.4)**

For this application the circuits FZH 161 and FZH 181 with open collector terminals are especially suited. Depending on the number of possible wired-AND-linkages at the output and on the numbers of inputs connected to them, the load resistors R_{TTL} amd R_{LSL} have an upper and lower limit value between which the resistance will range (cf. Siemens data book "Digital Integrated Circuits").

LSL – MOS-HV – LSL **(fig. 7.1.5)**

Because of their compatible levels LSL and MOS-HV circuits can easily be connected with the only exception that the usual negative MOS supply voltage must be displaced, as it has to happen to all systems shown up to **fig. 7.1.8**. LSL output and MOS input can be connected directly. The interface to a LSL input is different and depends on the condition of the MOS output. The output of the push-pull circuit ⑤ with a resistor of $R_{QL} \leqq 3$ kΩ (to V_{DD}) can be connected directly to the LSL input. Outputs according to ① with $R_{QH} \leqq 3$ kΩ require only a resistor connected to V_{GG} (see **fig. 7.1.5a**). In both cases only o n e LSL input can be operated (F_1 = 1). For MOS outputs with high impedances a transistor interface has to be provided. The circuit shown in **fig. 7.1.5b** applies to all MOS output stages which can supply currents of 0.1 mA and more. Currents of 0.5 mA and up can drive ten LSL inputs. For low switching speeds the resistor R2 can be dropped. The diode D is necessary only at output ④.

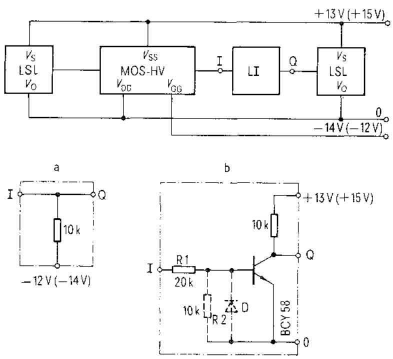


Fig. 7.1.5

LSL – MOS-LV – LSL **(fig. 7.1.6)**

In this example a TTL-compatible MOS circuit is a prerequisite. Since the level converter FZH 181 offers a TTL input, the same conditions apply as in **fig. 7.1.8**. The resistor R_{LSL} has to be dimensioned as in **fig. 7.1.4**.

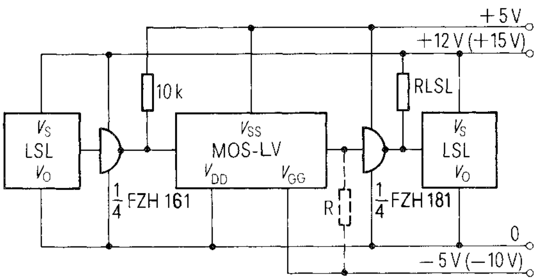


Fig. 7.1.6

TTL – MOS-HV – TTL **(fig. 7.1.7)**

For MOS outputs with $R_{QH} \leqq 1\ k\Omega$ the voltage divider consisting of R1 and R2 is sufficient. For low-ohmic push-pull outputs with $R_{QH} \leqq 200\ \Omega$ and $R_{QL} \leqq 1\ k\Omega$ a voltage divider with $R_1 = 360\ \Omega$ and $R_3 = 300\ \Omega$ is also possible. These values apply only for a TTL input. For larger loads or MOS outputs with higher impedances a transistor stage as shown in **fig. 7.1.5 b** has to be provided. The collector has to be connected to +5 V.

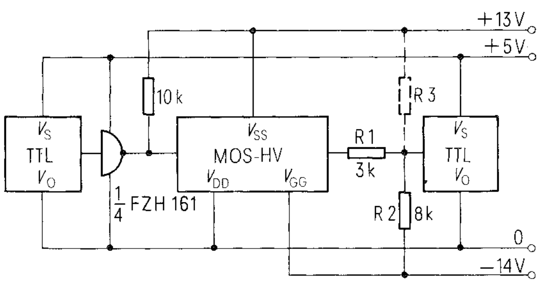


Fig. 7.1.7

TTL – MOS-LV – TTL **(fig. 7.1.8)**

Many MOS-LV as well as CMOS circuits with push-pull outputs are fully TTL-compatible and do not require any interface. Often these circuits are designed in saturated technique, i.e. with only one supply voltage V_{DD} whose value, refered to $V_{SS} = +5$ V, ranges normally between –5 and –10 V. For circuits according ① an external resistor R is sufficient. For outputs with high impedances and large TTL load a transistor stage has to be provided.

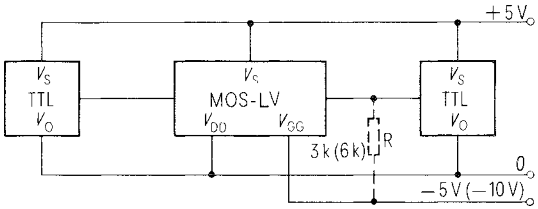


Fig. 7.1.8

LSL (TTL) – MOS-HV – LSL (TTL) (**fig. 7.1.9**)

If a displacement of the supply voltages is not possible, as demonstrated in the above mentioned examples, the circuit shown in **fig. 7.1.9** can be used as interface to MOS-HV systems. Depending on whether the interface is intended for LSL or TTL the corresponding values given in table 4 have to be used. Basically the same circuits apply to MOS-LV and CMOS.

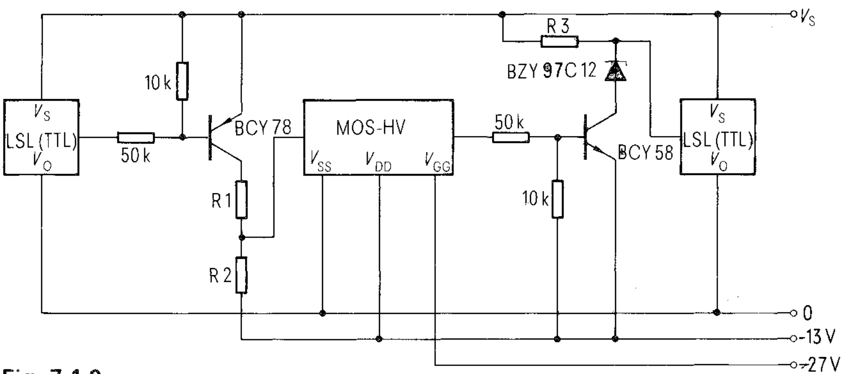


Fig. 7.1.9

Table 4

	V_S V	R1 kΩ	R2 kΩ	R3 kΩ
LSL	+12	10	10	20
TTL	+ 5	1	2.5	10

Clock generator and its interface

Fig. 7.1.10 and **7.1.11** demonstrate how a two-phase MOS clock generator can easily be realized with LSL or TTL circuits. Feedback-inverters generate the basic clock pulses, from which the two exactly separated clock pulses Φ 1 and Φ 2 are derived by using a divider and a linkage logic (cf. pulse diagram). MOS clock inputs often require higher levels than logic inputs and as shown in **fig. 7.1.10** levels corresponding to LSL-output levels of 12 to 14 V are achievable.

With the TTL-version higher clock pulse levels are possible, e.g. 27 V for MOS-HV. The reference levels have to be established in accordance with the forementioned examples.

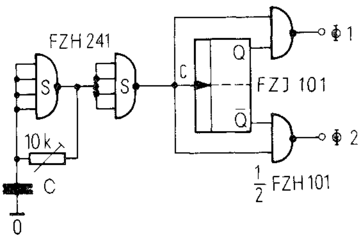
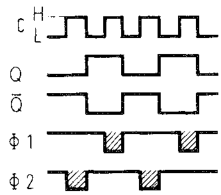


Fig. 7.1.10



pulse diagram for fig. 7.1.10 and 7.1.11

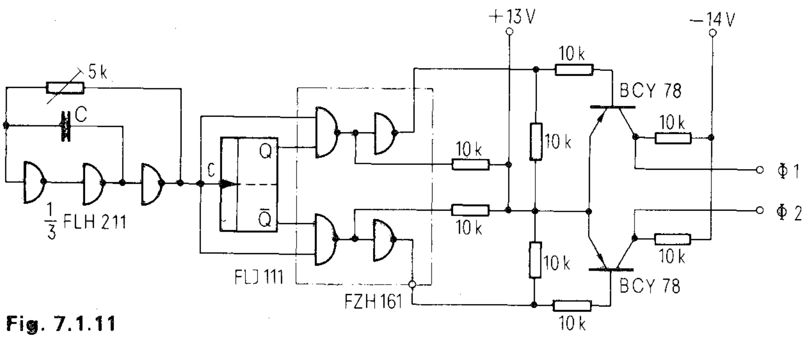


Fig. 7.1.11

7.2 Universal timing and counting circuit

The MOS-circuit SAJ 341 is a counter with preselection. By means of its programme-logic inputs different functions are possible, e.g. decimal counter or clock counter. Therefore this circuit is universally suited for counting applications as well as for timing. **Fig. 7.2.1** shows the block diagram of the SAJ 341 for the internal and external circuits. Both operations are characterized by fundamental and common functions, described in the following.

Function of operation

A 4-digit decimal counter and a divider connected in series are the principal items of the SAJ 341. Eight different operations can be selected by means of the programme logic having three dual-coded inputs I_{p1} to I_{p3}. These operations are classified into 2 groups: a) 5 decade counting operations, which differ by the ratio of the divider and b) 3 timing ones, which are different by the choice of set time bases. If this circuit is used as a clock, it operates as a 24-hour counter with read out of minutes and hours.

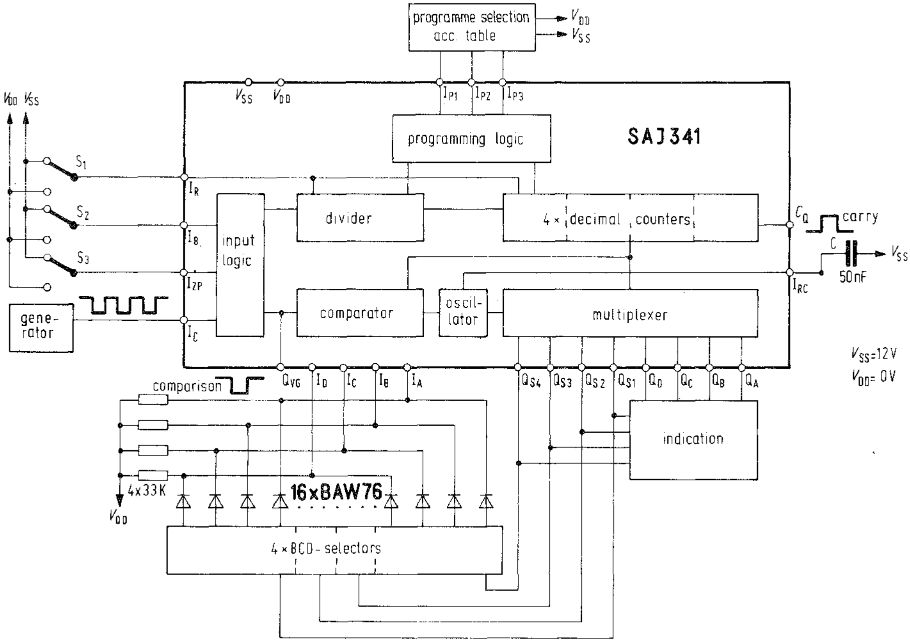


Fig. 7.2.1

The functions are described in the following table:

L-signal = V_{DD}-potential, H-signal = V_{SS}-potential

Program	Inputs I_{P3}	I_{P2}	I_{P1}	Functions
1	H	H	L	4 decimal counter
2	H	L	H	4 decimal counter with predivider 10:1
3	H	L	L	4 decimal counter with predivider 100:1
4	L	H	H	4 decimal counter with predivider 1000:1
5	L	H	L	4 decimal counter with predivider 6000:1
6	L	L	H	clock for time standard 20 ms or 50 Hz
7	L	L	L	clock for time standard $16^2/_3$ ms or 60 Hz
8	H	H	H	clock for time standard 10 ms or 100 Hz

Each digit output signal of the 4-digit decimal counter is obtained in parallel at the outputs Q_A to Q_D, whereby the digit place is defined at one of the selection outputs Q_{S1} to Q_{S4} as follows:

Table 2: L-Signal = V_{DD}-Potential, H-Signal = V_{SS}-Potential

selection outputs				digit place at	
Q_{S1}	Q_{S2}	Q_{S3}	Q_{S4}	counting operation	clock operation
H	L	L	L	1	1 min.
L	H	L	L	10	10 min.
L	L	H	L	100	1 hour
L	L	L	H	1000	10 hours

The output of the four digits is serially achieved and is cyclically repeated (time-division multiplex system). The frequency of the output cycle is determined by the internal oscillator, which require for its operation a 50-nF-capacitor, connected to terminal I_{RC}. Thus the oscillation frequency is typ. 100 kHz. If several SAJ 341 are operated synchronuously, an external signal with a frequency of 100 kHz can be applied to the input I_{RC}.

The selection outputs Q_S are also required for choosing the digit of the BCD-preselector inputs I_A to I_D. The input digit place is according to table 2. If the decimal counter has reached the predetermined number, a signal is available at the comparator output Q_{VG} = H. The counter is not allowed to run during the comparison, i.e. the pulse frequency at the clock input I_T has to be 10 times lower (about 10 kHz) than the one of the internal oscillator.

The preselector information has to be read in inversely to the required output information, i.e. for, e.g., $Q_D\ Q_C\ Q_B\ Q_A$ = HHLL $\triangleq$ decimal 3 it has to be $I_D\ I_C\ I_B\ I_A$ = LLHH.

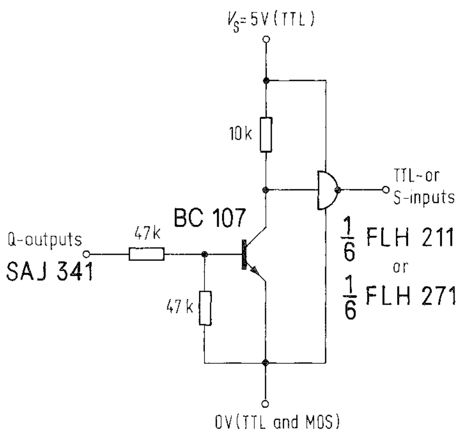


Fig. 7.2.2

The SAJ 341 operates also without a BCD-selector, if the inputs I_A to I_D are connected directly to V_{DD}-terminal. Without any preselector-operation the max. input frequency is only determined by the cut-off frequency of the decade counter or divider. It is typ. 50 kHz. By means of the carry output C_Q it is possible to connect the ICs in series.

Input I_R and an input logic with the inputs I_B and I_{ZP} allow additional functions, which have a different meaning for counting or clock operation.

When the supply voltage is applied, counter as well as divider are reset to L-signal by an internal reset process.

The following devices, indication, selectors, programme-selection, generator, RC-circuit and the pushbuttons S_1 to S_3 are connected externally to the SAJ 341. The indicator has to be dimentioned for time-division multiplex operation, which can be achieved by the following circuit. A MOS-TTL level interface stage according to **fig. 7.2.2** is additionally required for each output, assuming the voltages $V_{SS} = 12$ V and $V_{DD} = 0$ V, which are better suited for a TTL interface. Between the outputs Q_A to Q_D and the decoder inputs A to D of FLL 121 the inverter FLH 211 has to be connected. For driving the time-division multiplex inputs S_1 to S_4 via the outputs Q_{S1} to Q_{S4} the inverter with open collector output, type FLH 271, must be used.

Four BCD-selectors allow a certain set of the device for counting or clock operation. The inputs of the selector are connected with the selection outputs Q_S for choosing the digit. Thus the correct identifying of a BCD-information, corresponding to a digit, is attained.

The thumbwheel switch, type V42264-D14-A011, with four making contacts each is suitable as selector switch. The 33-kΩ-resistors provide the inputs I_A to I_D with a defined L-signal when the contacts are open.

The programme selection is achieved according to table 1. When required the following devices are suited: BCD-selector switch with 2 inputs and 8 positions, programme plug or fixed connections.

Counting, programme 1 to 5.

The device operates as a decimal counter with programmable divider. Pushbuttons at the inputs I_R, I_B and I_{ZP} enable the following functions:

L-signal at the reset input I_R sets the counters and dividers to L and blocks the clock pulse. The counter is enabled by a H-signal. This pushbutton allows to control the begin of the counting.

H-signals at the input I_B block the clock pulse input I_T. It is enabled by a L-signal. This function is for the start-stop operation, since the counter information is maintained.

L-signal applied to I_{ZP} : If the decimal counter has reached the predetermined figure, a H-signal is available at the following comparator output Q_{VG}. This H-signal changes to L with the clock pulse. The counting is continued. This operation is favoured for, e.g., pulse selecting circuits, programmable decimal frequency dividers, dividers in general etc.

H-signal at I_{ZP} : If the decimal counter has reached the preset figure, the comparator output Q_{VG} changes to H-signal. The clock pulse is internally blocked, the counter remains on the preset value and Q_{VG} continues in staying on H-level. This function is favoured for applications with defined counting sequences. The counter runs self-locked. A new operation begins either by a resetting or by a signal change at I_{ZP}.

In general the SAJ 341 is applicable as counter for quantities and for operating hours as well as totalizing counters up to a capacity of 6×10^6 units.

The carry output C_Q changes to L-signal at a counter position of decimal 8000 and returns to H-level when the counter changes from decimal 9999 to 0000.

Clock operation, programme 6 to 8

The IC operates as a 24-hour-clock, displaying minutes, with 3 different time bases of frequency standards. Programme no. 6 is intended for generator pulses with a duration of 20 ms, which are derived from the mains frequency of 50 Hz. Programme 7 is similarly suited for operations locked to a mains frequency of 60 Hz. Programme 8 is favoured for cristal controlled operations at 100 kHz, for instance. Whereby the required input frequency of 100 Hz for the SAJ 341 can be obtained through an additional divider of 1000 : 1, type SAJ 131.

The BCD-selectors serve firstly for setting the clock and secondly for preselecting a defined time for clock switch or alarm clock operation. The pushbuttons S_2 and S_3 shown in **fig. 7.2.1** are not used at this application. S_1 is the set-pushbutton, whereby applies:

S_1 to V_{SS}, I_P = H: setting to a preselected time

S_1 to V_{DD}, I_R = L: clock operation

The reset of the clock to 0 h 0 min can be achieved by interrupting shortly the connection to one of the power supply lines.

The comparator output Q_{VG} supplies a pulse with a duration of 1 min for alarm or switch operations when the preselected time has been reached. By this means the following functions can easily be realized: circuits for delay time operations, for preset-time control and for timing.

Simple clock applications do not require a preselection. The pushbuttons S_1 to S_3 have the following functions at this operation:

S_1: resetting the clock to 0 h 0 min

S_2: setting the minutes

S_3: setting the hours

S_1, S_2, S_3 to V_{SS} : I_R = I_B = I_{ZP} = H: clock operation.

If S_2 and S_3 are pushed, always single pulses are produced. They affect the minute-counter and the hour-counter via the inputs I_B or I_{ZP}. In order to avoid this disadvantages the pushbuttons have to operate without any chatter. The clock pulse line is interrupted during the setting operation.

The carry output Q_C supplies the carry for the next day. It changes from L-signal at 22 : 00 and returns to H-level when the clock shifts from 23 : 59 to 24 : 00 (display 00 : 00).

7.3 7-segment display for time-division multiplex operation

Light emitting diodes are more and more used as displays in electronic devices due to their favourable features. On account of their high switching frequency and of their extremely simple driving circuit LEDs are ideal elements for pulse operations. **Fig. 7.3.1** shows for this application a circuit of a 4-digit display for time-division multiplex operation.

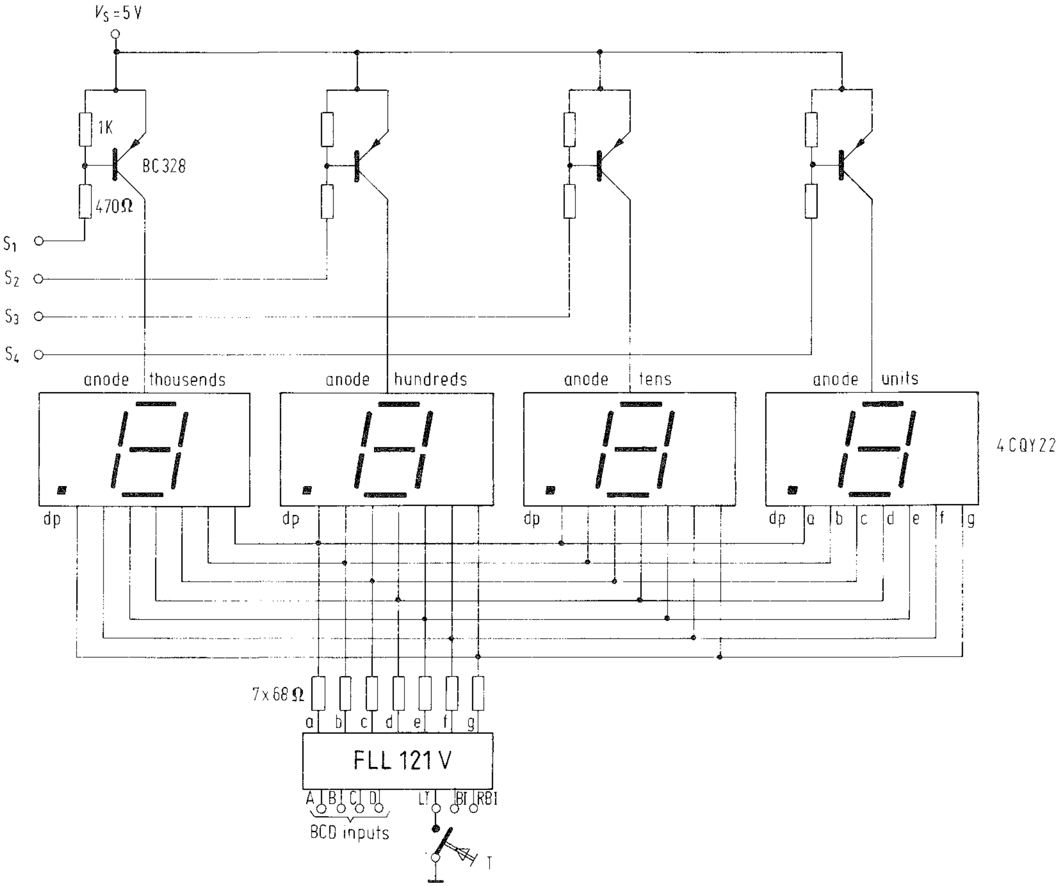


Fig. 7.3.1

This unit is mainly applicable for higher integrated chips which include already a multiplex system. In this case only an appropriate TTL-level interface has to be established.

The integrated circuit FLL 121 converts the BCD-information, supplied to the inputs A, B, C, D, to the 7-segment code and drives the display CQY 22. The 68-Ω-resistors limit the current to the admissible value of 40 mA for each output. The pushbutton T, connected to the input LT, enables the operation of all seven segments for checking the CQY 22. The inputs BI and RBI serve for the zero-signal extraction, if several decoders are used.

The digit selection is obtained at the inputs S_1 to S_4 via the transistors BC 328. The S-inputs can be driven directly by any TTL-device with open collector output.

If more than 4 displays CQY 22 are operated by the driver FLL 121, the light intensity of the display is disadvantageously reduced. The average current *i* for each segment is achieved by the following equation:

$$i = \frac{I_Q}{n} = \frac{40}{4} = 10\ \text{mA},$$

whereby I_Q is the permissible output current of the FLL 121 V and n is the number of digits.

The current calculated above is sufficient to guarantee a required light intensity of 100 to 200 μcd at normal conditions.

Fig. 7.3.2 shows the total circuit of the display unit with time-division multiplexer and input multiplex system for 4 counters. The Schmitt-trigger FLH 351 operates as clock pulse generator. Its frequency can be nearly linear varied in a range of 10 Hz to 10 MHz through the capacitance of the capacitor C. In order to achieve a safe beginning of the oscillation the resistance of R should not exceed a value of 330 Ω.

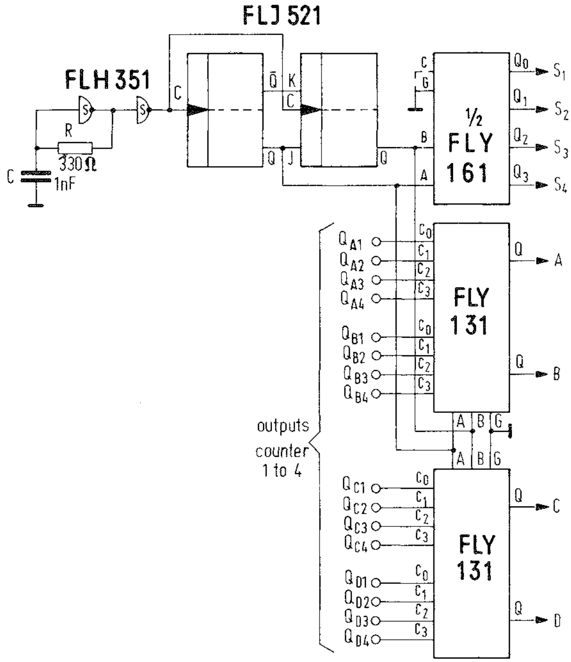


Fig. 7.3.2

The flipflop FLJ 521 serves as a binary divider and produces the signals required for the selection inputs A and B of the multiplexers FLY 131 and FLY 161. The information inputs C_0 to C_3 of the two input multiplexers FLY 131 are connected with the outputs Q_A to Q_D of the counters 1 to 4 as shown in the figure. They achieve a synchroneous switching of counter outputs and digits. The IC FLY 161 produces the signals required for digit selection at S_1 to S_4. According to the used circuit part the input C of the FLY 161 is connected to L or H-level. The current at S_1 to S_4 is proportioned with 8 mA each, corresponding to a standard TTL-load factor of $F_Q = 5$. Thus each Q-output of the FLY 161 can drive two S-inputs of displays being independent on each other.

The following truth table applies for the circuit:

Selector-inputs		Outputs							
A	B	S_1	S_2	S_3	S_4	A	B	C	D
L	L	L	H	H	H	$Q_{A\,1}$	$Q_{B\,1}$	$Q_{C\,1}$	$Q_{D\,1}$
L	H	H	L	H	H	$Q_{A\,2}$	$Q_{B\,2}$	$Q_{C\,2}$	$Q_{D\,2}$
H	L	H	H	L	H	$Q_{A\,3}$	$Q_{B\,3}$	$Q_{C\,2}$	$Q_{D\,3}$
H	H	H	H	H	L	$Q_{A\,4}$	$Q_{B\,4}$	$Q_{C\,4}$	$Q_{D\,4}$

$Q_{A\,1}$, $Q_{B\,1}$ etc. means in the third column that the potential of the indicated output is applied to A to D.

7.4 Universal code converter

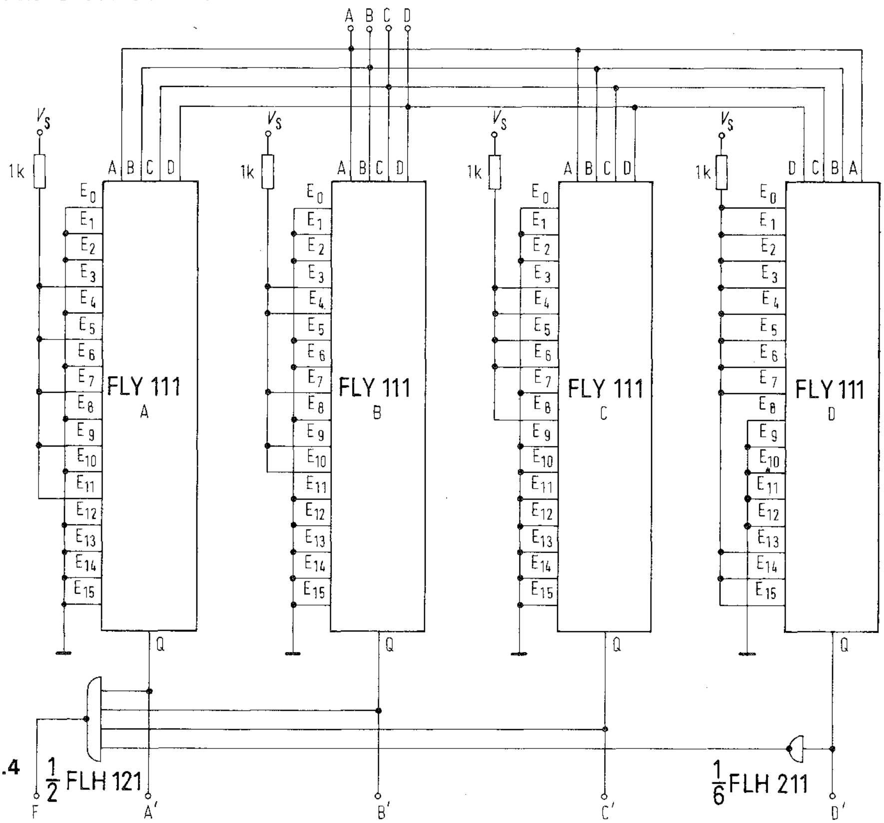


Fig. 7.4

Fig. 7.4 shows a programmable code converter for 4 bit with the selector-IC, type FLY 111. The circuit is particularly favoured at high converting speeds or when a fast matching to codes of other systems is required. The code which is to be converted is supplied in parallel to the selector inputs A to D of the FLY 111. Always one of the information inputs E_0 to E_{15} is connected with the output Q. The logic levels at E_0 to E_{15} can be freely chosen, therefore any code words can be used. To explain the function of the shown circuit a special code has already been determined.

The following table shows a summary of codes often used and their allocation to the dual system.

Table 1:

Chosen information input	Dualcode = code word at selector input				corresponding decimal figure at				
	D	C	B	A	Dual code	2-4-2-1 code	Aiken-code	Exceß-3-code	Gray-code
all of E_0	L	L	L	L	0	0	0	–	0
all of E_1	L	L	L	H	1	1	1	–	1
all of E_2	L	L	H	L	2	2	2	–	3
all of E_3	L	L	H	H	3	3	3	0	2
all of E_4	L	H	L	L	4	–	4	1	7
all of E_5	L	H	L	H	5	–	–	2	6
all of E_6	L	H	H	L	6	–	–	3	4
all of E_7	L	H	H	H	7	–	–	4	5
all of E_8	H	L	L	L	8	–	–	5	15
all of E_9	H	L	L	H	9	–	–	6	14
all of E_{10}	H	L	H	L	10	4	–	7	12
all of E_{11}	H	L	H	H	11	5	5	8	13
all of E_{12}	H	H	L	L	12	6	6	9	8
all of E_{13}	H	H	L	H	13	7	7	–	9
all of E_{14}	H	H	H	L	14	8	8	–	11
all of E_{15}	H	H	H	H	15	9	9	–	10

The table is used for programming as follows:

e.g. Excess-3/Aiken-code converter

The chosen information inputs E are achieved as a function of the code word applied to A to D. If the concerned code word is BCDA = LHHL according to a decimal 3 of the excess-3-code, for instance, then all E_6-outputs are enabled. The programming of the logic levels results accordingly from a decimal 3 of the Aiken-code, i.e. DCBA = LL HH. It has to be considered that the information selector FLY 111 inverts the signal between input E and output Q, thus follows for $E_{6\,D}$ $E_{6\,C}$ $E_{6\,B}$ $E_{6\,A}$ = DCBA = HHLL. The non-required inputs E_0, E_1, E_2, E_{13}, E_{14} and E_{15} are expediently provided with an error detection code. Suitable code words are non-existing dual combinations as, e.g., D'C'B'A' = E = LHHH. The NAND-gate FLH 121 in combination with the inverter FLH 211 indicates the error by a signal change from H to L at the output F.

The total function table of the code converter according to **fig. 7.4** is as follows:

Table 2:

Dec.	Inputs (Exceß-3-code) D	C	B	A	Outputs (Aikencode) D'	C'	B'	A'	Error detection F	Chosen information input E
0	L	L	H	H	L	L	L	L	H	E_3
1	L	H	L	L	L	L	L	H	H	E_4
2	L	H	L	H	L	L	H	L	H	E_5
3	L	H	H	L	L	L	H	H	H	E_6
4	L	H	H	H	L	H	L	L	H	E_7
5	H	L	L	L	H	L	H	H	H	E_8
6	H	L	L	H	H	H	L	L	H	E_9
7	H	L	H	L	H	H	L	H	H	E_{10}
8	H	L	H	H	H	H	H	L	H	E_{11}
9	H	H	L	L	H	H	H	H	H	E_{12}
Error	L	L	L	L	L	H	H	H	L	E_1
Error	L	L	L	H	L	H	H	H	L	E_2
Error	L	L	H	L	L	H	H	H	L	E_3
Error	H	H	L	H	L	H	H	H	L	E_{13}
Error	H	H	H	L	L	H	H	H	L	E_{14}
Error	H	H	H	H	L	H	H	H	L	E_{15}

The free programming of the circuit enables a lot of additional applications, such as code generators or sequence controls. A great advantage is achieved by the fact that the programme information cannot be lost by a power supply break down or by interference pulses. Therefore this circuits is suited as a programmable read-only memory. For these applications the selection of the programme step at the selector inputs A to D can be obtained through a 4-bit binary counter FLJ 181, for instance.

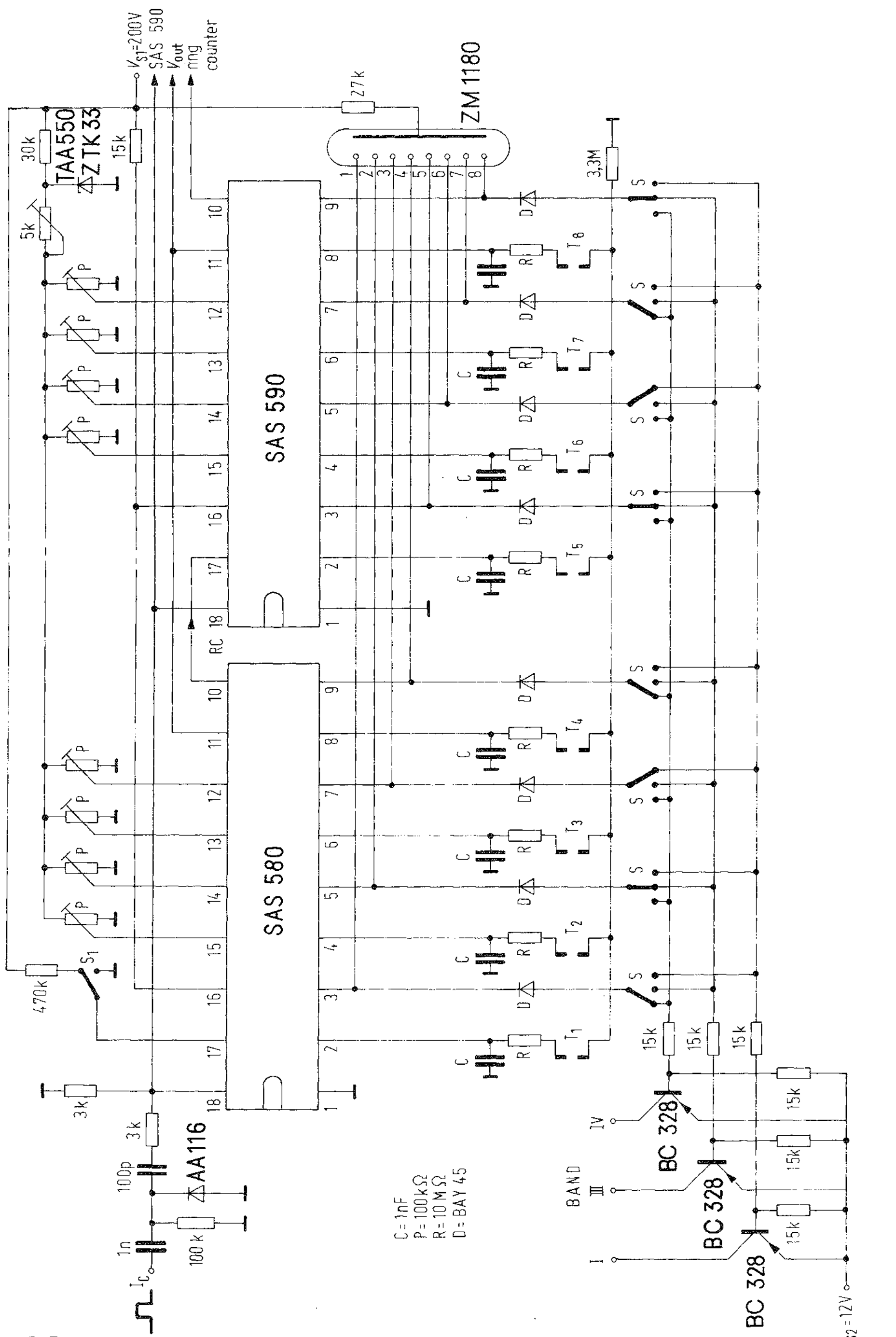
7.5 Channel selection with touch-keys

The integrated circuits SAS 580 and SAS 590 are designed for applications with touch-keys. They are especially favoured for electronic channel selection and **fig. 7.5** shows a memory circuit for 8 channels. The desired station is selected by touching one of the metallic sensor plates T_1 to T_4 at the SAS 580 and T_5 to T_8 at the SAS 590, whereby a previously selected channel is turned off by means of the interdependent coupling of the ICs at pin 18.

The integrated circuits SAS 580 and SAS 590 include additionally ringcounters for automatic step-by-step actions, which are achieved by pulses with an amplitude of 5 to 10 V_{pp}. These pulses have to be supplied to input I_Z and the switching is caused by each leading edge. The rise time has to be less than 1 μs, whereas the pulse duration is not limited. The step-on signal is supplied from one IC to the other through a connection between pin 10 of SAS 580 and pin 17 of SAS 590. If all stages have been passed the first one is automatically turned on. A step-on frequency up to 10 kHz is applicable.

The tuning voltage V_{out} can be adjusted through the potentiometers connected to terminals 12 to 15. The supply-voltage for these potentiometers is stabilized by the voltage regulator TAA 550. The tuning voltage is synchronously switched when one of the sensor plates is touched. It is available at the common lead connected to pin 11 of each IC.

The pins 3, 5, 7 and 9 are the open-collector terminals of the npn-output transistors, which switch synchronously, too. The permissible output current is 55 mA. This is sufficient to drive filament lamps, glow lamps or LEDs.



V_{S1}=200V
SAS 590
V_{out}
ring
counter
27k
ZM1180
30k
TAA550
ZTK33
15k
5k
3,3M
SAS 590
SAS 580
RC
470k
S_1
3k
3k
100p
AA116
1n
100 k
I_c
C = 1nF
P = 100 kΩ
R = 10 MΩ
D = BAY 45
BAND
IV
III
I
BC 328
BC 328
BC 328
15k
V_{S2}=12V

Fig. 7.5

In the circuit shown in **fig. 7.5** a nixie tube, type ZM 1180 is used. The mentioned outputs can also drive transistors for band switching, whereat the band selection is achieved by the selectors S, which are generally programmed only one time. During the reverse period of the output transistors the diodes BAY 45 protect the band switching transistors against the high voltage required to drive the nixie tube.

If a voltage of less than 0.5 V is applied to the input at pin 17 of the SAS 580, the sensor plates and the ring counter are blocked. As shown in **fig. 7.5** the switch S_1 is provided for this operation. It connects pin 17 to ground. The information of the channel previously selected remains stored, i.e. the circuit is also suitable for stand-by operation. In this case the supply voltage V_S may be reduced to a value of 12 V.

The number of channels is extended by adding any quantity of SAS 590. But it is permitted to use only one SAS 580, since it selects automatically channel 1 after applying the supply voltage. The terminals 18 and 11 are connected in parallel in the case of extension. A connection "RC" has to be made from one IC to the following one. If any digital display is used, an additional decoder is required.

The metallic sensor plates are connected in series with resistors of 10 MΩ and 3.3 MΩ to meet the VDE-standards for devices without any mains separation. The capacitor C suppresses eventual interferences, such as hum. The sensor plates should be designed in such a way, that a groove or any hollow is between the plates. Thus a constant bridging caused by dirt is essentially avoided.

7.6 Electronic scale with light emitting diodes

Digital scale indication by means of a moving light spot are particularly favoured to registrate approximate values, such as applications of, for example: car speedometer, petrol gauge, level indicator, tuning scales etc. For the application in measuring instruments a special region of the scale can be accentuated by using LEDs with different colours.

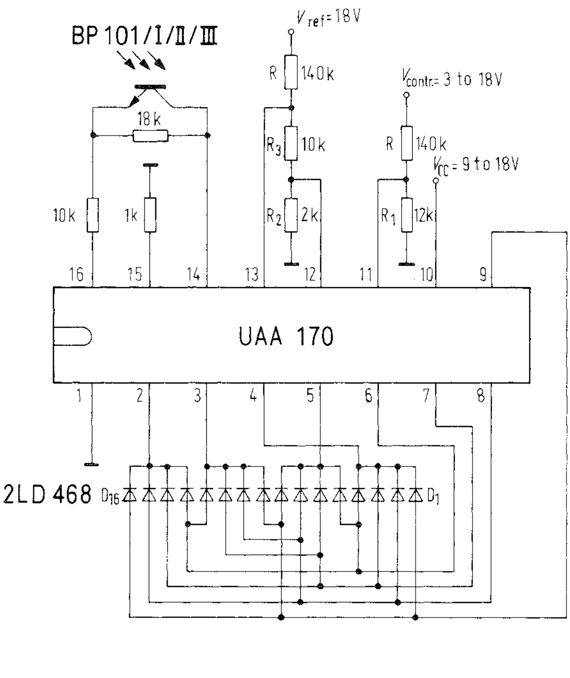


Fig. 7.6.1

The integrated circuit UAA 170 has especially been designed for driving a scale with 16 LEDs. The circuit is shown in **fig. 7.6.1**. The input voltages at pins 11, 12 and 13 can be freely chosen within a range of 0 and 6 V. For higher supply voltages (e.g. 18 V) suitable dividers have to be used. The dc level at pin 11 determines which one of the LEDs is turned on. The voltage difference $\Delta V_{contr.}$ for the step-by-step action depends on the reference voltage V_{ref} and is adjustable through its divider. The voltage difference $V_{R\,3}$ between pin 12 and 13 corresponds to the possible indication range. It determines also the changeover from one diode to the other. If the voltage is $V_{R\,3} \sim 1.2$ V, the light point moves smoothly and continuously along the scale. With increasing voltage difference, e.g. up to $V_{R\,3} \sim 4$ V, the light point moves more and more abruptly. At input voltages which do not correspond to those required for the indication range either the diodes D_1 or D_{16} are turned on. Therefore only the order of magnitude can be determined. The true value is detected only when the change-over occurs from D_1 to D_2. This value detection is discontinued when the change-over happens between D_{15} and D_{16}. The relation between reference voltage and control voltage is easily experienced when the voltage divider at the pins 11, 12 and 13 are identical.

Assuming $R_1 = R_2 + R_3$ and R_g = total resistance, then applies:

1. $\dfrac{V_{ref}}{V_{R\,3}} = \dfrac{R_g}{R_3}$,

2. $\dfrac{V_{ref}}{V_{contr,\,min}} = \dfrac{R_2 + R_3}{R_2} = 1 + \dfrac{R_3}{R_2}$,

3. $V_{contr,\,max} = V_{ref}$.

From the equation 3 follows that control and reference voltage have to have the same value, e.g., $V_{contr,\,max} = 18\text{ V} = V_{ref}$. The desired voltage difference ΔV_{contr} for the step-by-step action determines the minimum control voltage $V_{contr,\,min} = V_{contr,\,max} - 15\,\Delta V_{contr.}$. If ΔV_{contr} is 1 V, then it is $V_{contr,\,min} = 3$ V. Thus the following resistance ratios are achieved

at smooth change-over:

$$\frac{R_g}{R_3} = \frac{18}{1.2} = 15$$

$$\frac{R_3}{R_2} = \frac{18}{3} - 1 = 5$$

at abrupt change-over:

$$\frac{R_g}{R_3} = \frac{18}{4} = 4.5$$

$$\frac{R_3}{R_2} = \frac{18}{3} - 1 = 5$$

The divider current should be dimentioned so that the input current of the UAA 170, being in the range of some μA, is negligible. Good average values are $I \sim 100\ \mu$A or $R_g \sim 150$ kΩ. Thus follows for the resistances under consideration of standard values:

at smooth change-over:

$R_3 = 10$ kΩ
$R_2 = 2$ kΩ
$R_1 = 12$ kΩ
$R = 140$ kΩ

at abrupt change-over:

$R_3 = 33$ kΩ
$R_2 = 5.6$ kΩ
$R_1 = 39$ kΩ
$R = 110$ kΩ

For the indication applies:

diode	D_1	D_2	D_3	...	D_{14}	D_{15}	D_{16}
value of V_{contr} =	< 4	4	5	...	16	17	> 17 V

The diodes are connected according a matrix, i.e. only 8 control leads are required. Each quartet has to consist of diodes with the same characteristics to achieve a correct operation. Therefore it is possible to have, for example, for the first and forth quartet red diodes and for the second and third green ones, in order to emphazise a special operating range.

Through the resistors connected to pins 14, 15 and 16 the LED-current can be adjusted in a range of $I_F \sim 0$ to 50 mA in accordance to the desired light intensity. The 1-kΩ-resistor defines the control range. The resistor connected between pin 14 and 16 determines the current. **Fig. 7.6.1** shows a circuit at which this resistor is replaced by a phototransistor BP 101. Thus the brightness of the LEDs can be matched automatically to the ambient light intensity. In this case the diode current ranges between $I_F \sim 5$ mA at a non-illuminated BP 101 and $I_F \sim 50$ mA at total illumination. Without a phototransistor a fixed resistor is sufficient. It should have a resistance of about 10 kΩ at $I_F \sim 50$ mA and of about 40 kΩ at $I_F \sim 0$ mA.

Fig. 7.6.2 shows an extension of the circuit to 30 diodes by using two UAA 170. The diodes D_{16} or D_{17} are turned on continuously, when the mutual limits are exceeded. If required they have to be switched off. The reference voltage $V_{R\,3} = 2 \times 1.2\ \text{V} = 2.4\ \text{V}$ is derived from a regulated dc voltage of typ. 5 V, which is available at pin 14. A 6.2-kΩ-resistor archieves an overlapping of the ranges in order to guarantee a smooth change-over from D_{15} to D_{18}. The control voltage $V_{contr.}$ is supplied in parallel to pin 11 of each IC via the divider R : R_1. The voltage divider has to be proportioned according to the desired input voltage. If a divider current of $I = 100\ \mu\text{A}$ and a control voltage of $V_{contr} = 10$ V are assumed, the resistances are as follows:

$$R_1 = \frac{V_{ref}}{I} = \frac{2.4}{0.1} = 24\ \text{k}\Omega, \qquad R = \frac{V_{contr} - V_{ref}}{I} = \frac{7.6}{0.1} = 76\ \text{k}\Omega$$

According to standards a value of R = 75 kΩ is chosen. The voltage difference for the step-by-step action is in this case: $\Delta V_{contr} = 10\ \text{V} : 30 = 0.16\ \text{V}$.

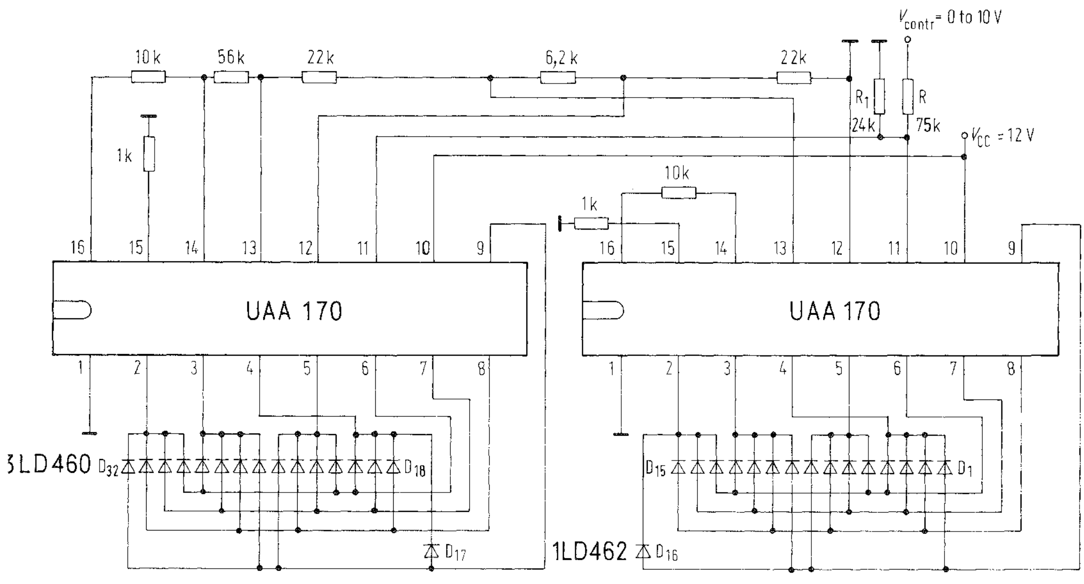


Fig. 7.6.2

The UAA 170 is also suitable for applications with less than 16 diodes. The only difference is that the diode quartets have to be replaced by single LEDs connected between V_{CC} and pins 2, 3, 4 and 5.

4 diodes: one each between pins 2, 3, 4, 5 and V_{CC},
5 diodes: one quartet to pin 2, one diode between V_{CC} and connected pins 3, 4 and 5,
9 diodes: one quartet each to pins 2 and 3, one diode between V_{CC} and connected pins 4 and 5,
13 diodes: one quartet each to pins 2, 3 and 5, one diode between pin 4 and V_{CC}.

7.7 Dynamic noise immunity of LSL-elements

The special feature of the LSL-series FZ 100 is the possible addition of capacitors at the N-terminal. This capacitor C_N acting as a Miller-integrator extends the delay times. Thus the dynamic noise immunity can easily and quickly be matched to the requirements of the installation side. In most cases it is sufficient to add delaying capacitors only at the input gates as shown in **fig. 7.7.1a**. The control section remains without any delay capacitors.

Under the prior condition of a slow switching characteristic, as shown in **fig. 7.7.2a**, the main task of the input logic is to separate the noise of the input signals as well as to keep it back from the system. The active duration of any noise is much shorter than the propagation delay. Thus any reaction is excluded.

The control system has to process the information, whereby the required operating speed is determined by the timing of the input signals at I_1 and I_2. Compared to the input logic the system has in general to operate much faster.

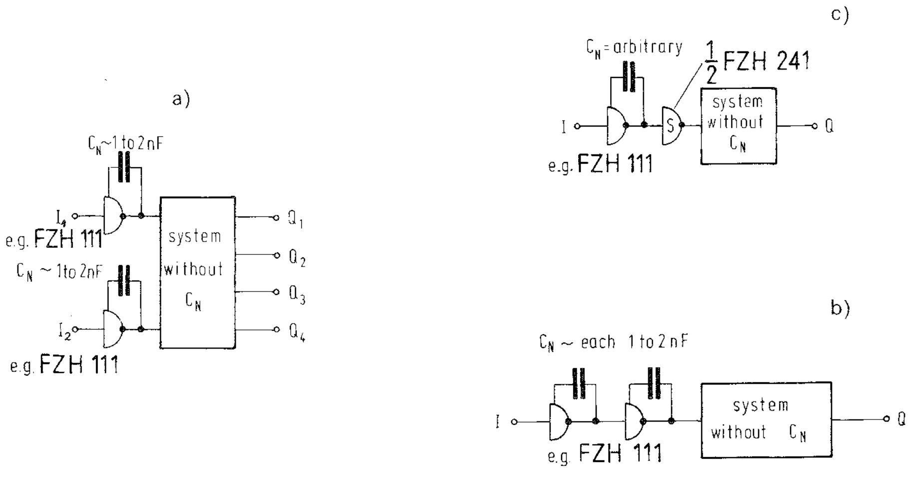


Fig. 7.7.1

Interfacing slow-operation input circuits with fast systems can cause problems unless the transition time of control pulses is sufficiently short. The threshold value is very critical, as in its vicinity the noise immunity is greatly reduced. The probability of any noise pulse interference is the greater the slower the threshold is passed by the incoming signal.

Fig. 7.7.2 demonstrates how various circuits react to such noise pulses in the vicinity of the threshold V_S. Fig. 7.7.2 a shows a slow input pulse with interfering noise spikes, which cause a negligible dip only during the threshold transition (see fig. b). All other noise is eliminated and has no influence, since the Schmitt-trigger does not react due to its different on and off threshold values V_{So} and V_{Su}. In fig. c the reaction of other circuits as flipflops, counters and registers is shown. If the above mentioned input signal is used as a clock pulse, a noise spike during the threshold transition V_S may lead to premature termination of the clock pulse. Assuming that this operation happens also during the trailing edge of the input signal, a counter will not increment according to one clock pulse but to three. Fig. d demonstrates the reaction of a timing circuit, if a noise spike occurs at the threshold transition of the trailing edge, i.e. an additional pulse is generated. However, the output pulse duration t_Q has to be shorter than the one of the input pulse.

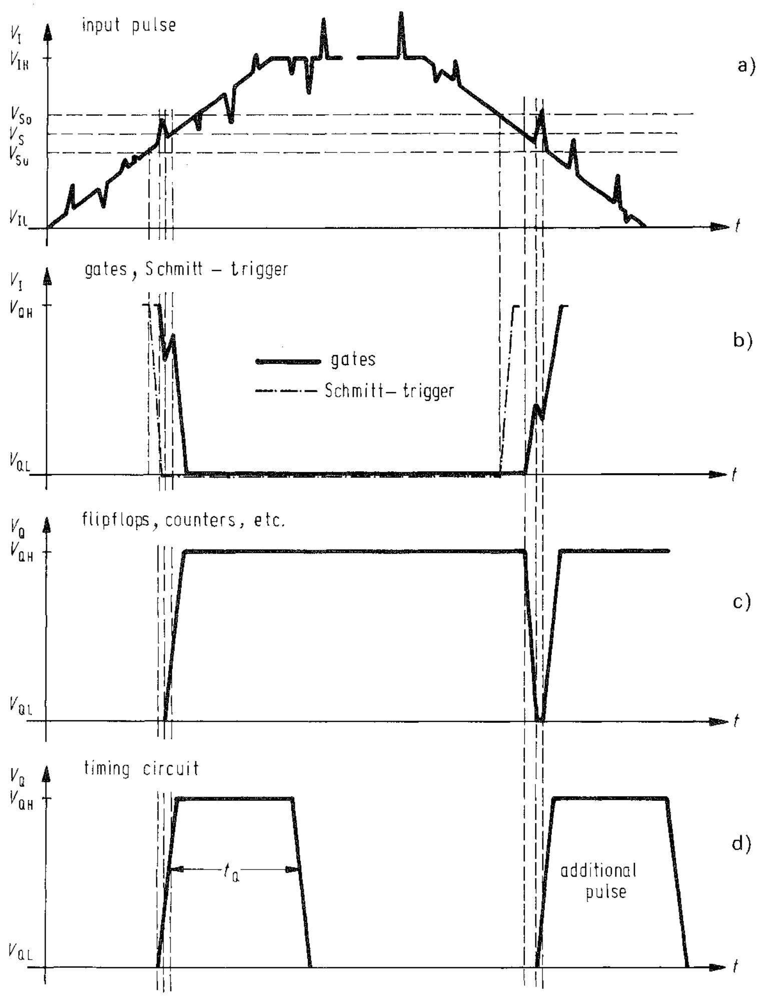


Fig. 7.7.2

The problems described apply basically to any system interface. Therefore it can be postulated that any interface circuit must also match the transition time adequately. The probability of errors caused by noise is small, if the threshold transition is accomplished rapidly. In particular for LSL-series the following conclusions may be drawn.

1. The additional capacitors C_N should have always the same capacitance within a system.
2. If circuits with and without capacitance are combined, the capacitor of the interface gate should not exceed a value of C_N = 1 to 2 nF, which is sufficient to suppress noise pulses up to a duration of 10 to 20 μs **(fig. 7.7.1a).**
3. For circuits with higher additional capacitances a pulse former is required. In this case the Schmitt-trigger FZH 241 is especially favoured and arbitrary capacitances may by applied to circuits infront of the FZH 241 as shown in **fig. 7.7.1b.**
4. **Fig. 7.7.1c** shows another possibility of noise elimination by means of additional capacitors. Noise during threshold transition can pass only the first stage, whereby its propagation delay causes a threshold transition delay of the second stage so that any such noise is safely eliminated.

7.8 Alphanumeric display with character generators

For displays consisting of a LED-matrix normally a device with 35 dots (5×7) is used to present the alphanumeric characters. To select a single diode of any character the read-only memory MK 2302 is especially suitable, since the information once set can be read nondestructively as often as required. The circuit shown in **fig. 7.8** is an example for an application of an one-digit display. With input memories in addition the character generator will be able to deliver characters for a minimum of four digits.

Circuit description

The information saying which of the 64 characters has to be indicated is set via inputs 1 to 6 by using a 6 bit ASC II-code (TTL-level). The selected character of the ROM is now read column by column. A 500 Hz-generator (FLH 101) switches column by column the character generator (pin 7) as well as the shift register FLJ 441 (pin 8) and selects the column sequentially blanked. The column-address is read in the shift register via the series inputs 1 and 2 and out via parallel outputs $Q_A \ldots Q_E$. The parallel output Q_F is connected to the reset input R via an inverter. By that the 8-bit shift register is reset after 6 clock pulses (5 columns and one blank clock pulse.) The character generator is reset automatically after each sixth clock pulse.

The lines of the LED-matrix are controlled by the character generator and the columns by the shift register. As the output current of both circuits is not able to drive the light emitting diodes, seven transistors BC 257 are connected between character generator and matrix. Between shift register and matrix a driver stage 75492 is used for the same reasons. The diode current is determined by the resistors having a value of 68 Ω each.

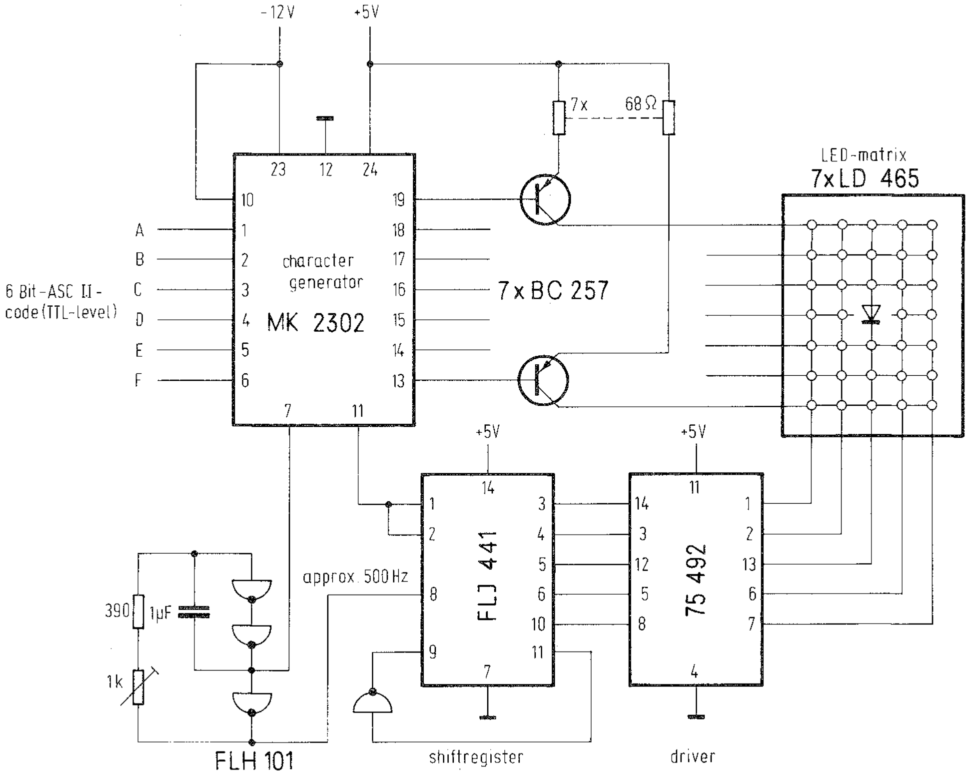


Fig. 7.8

Operating conditions

Mean diode current	about 6 mA
Peak current per diode	about 35 mA
Peak current per column	max. 250 mA

Total current consumption

5 V-supply: 80 to 170 mA
(depends on character chosen)
12 V-supply: 25 mA